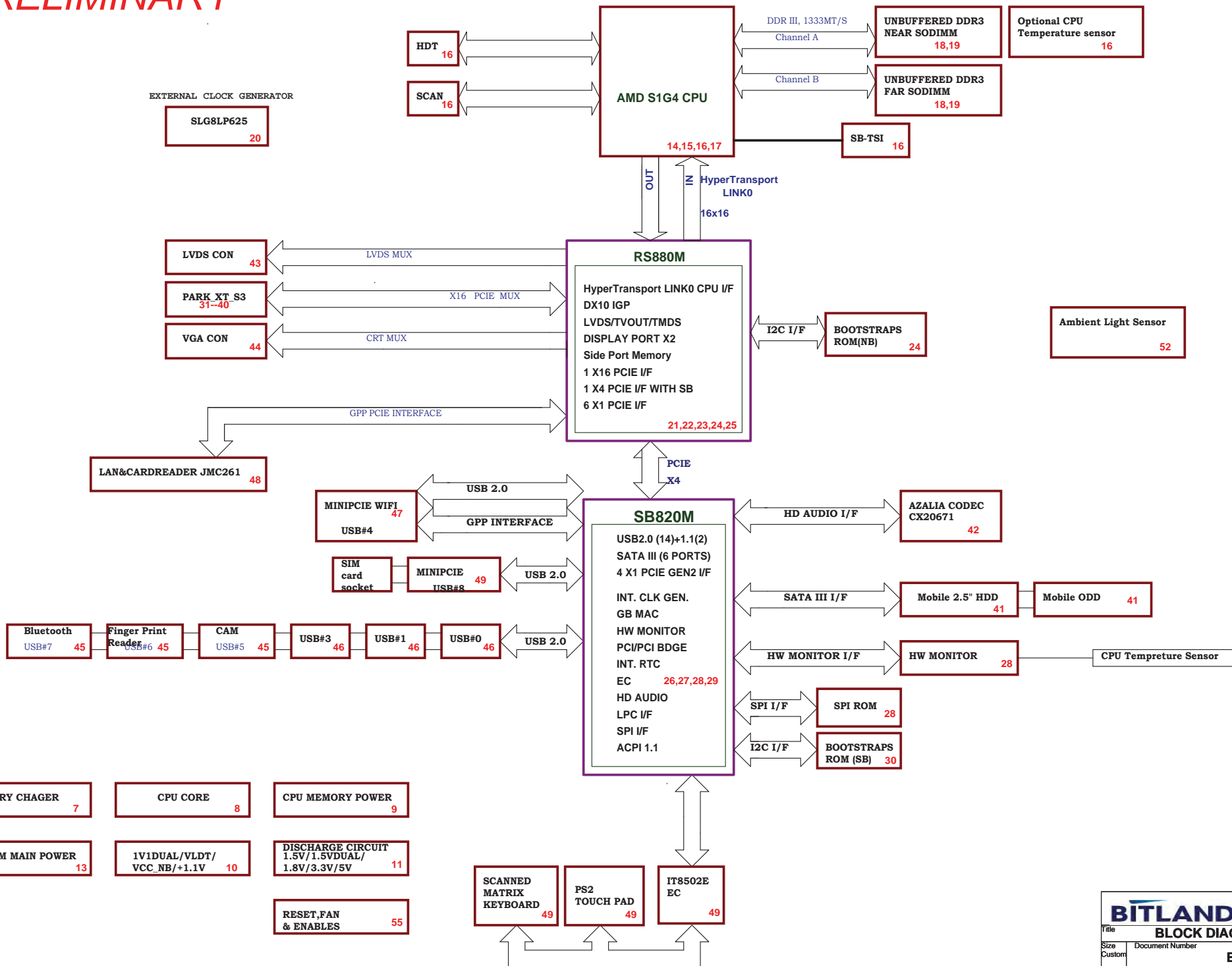


PRELIMINARY

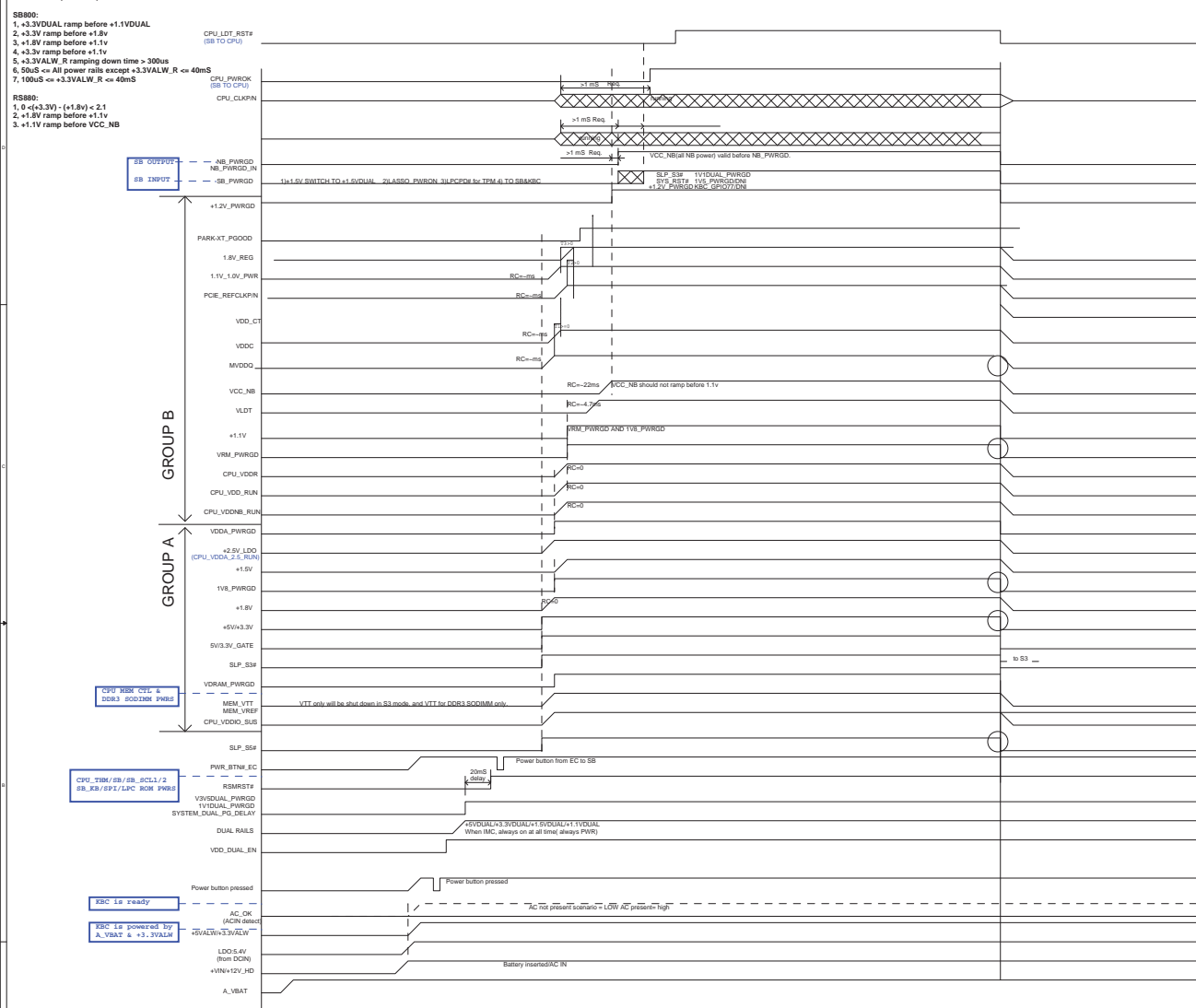
# GUAM S1G4 SCHEMATIC DESIGN



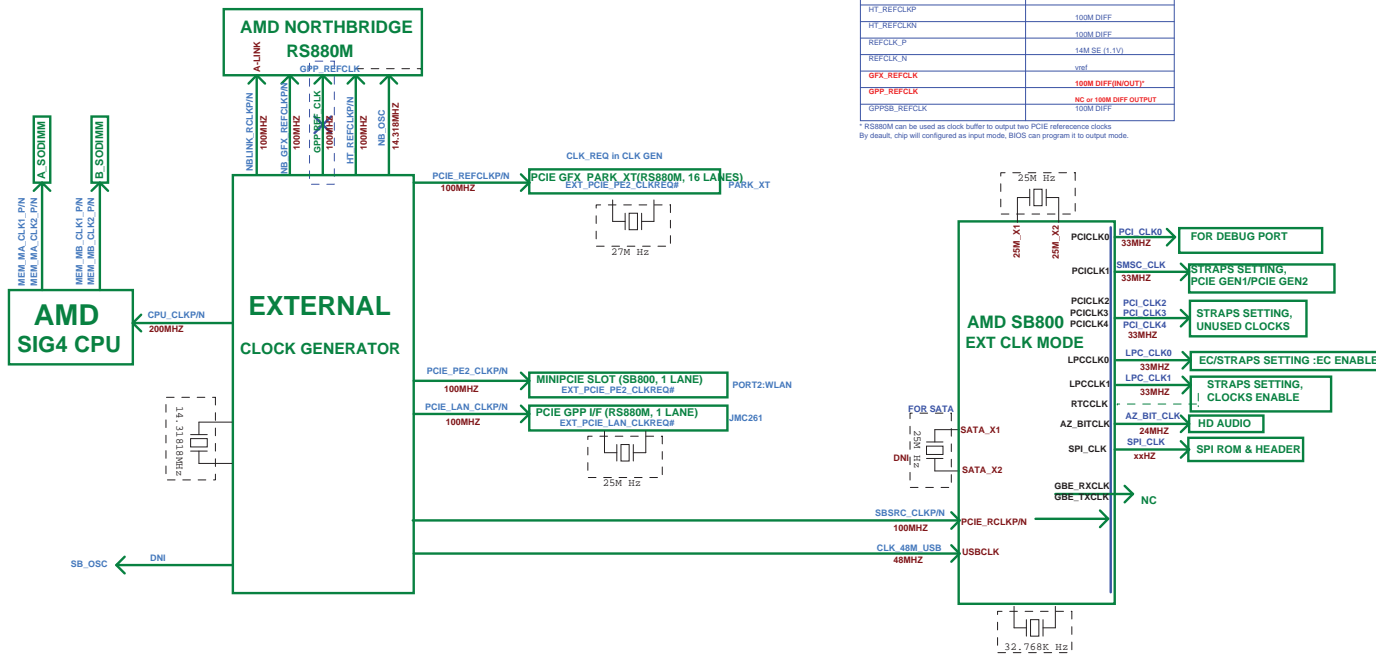
# TABLE OF CONTENTS

<b>BITLAND</b>		Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
<b>TABLE OF CONTENTS</b>			
Title	Document Number		Rev
Size	<b>BM5016</b>		1.0
Custom			
Date:	Thursday, August 05, 2010	Sheet	2 of 54

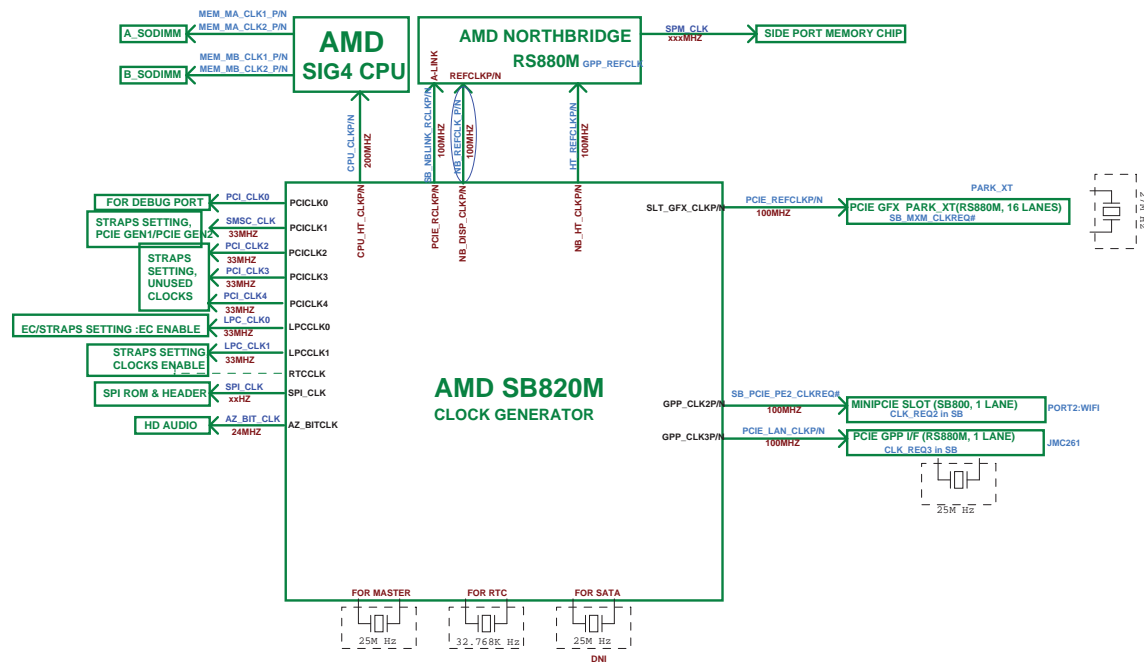


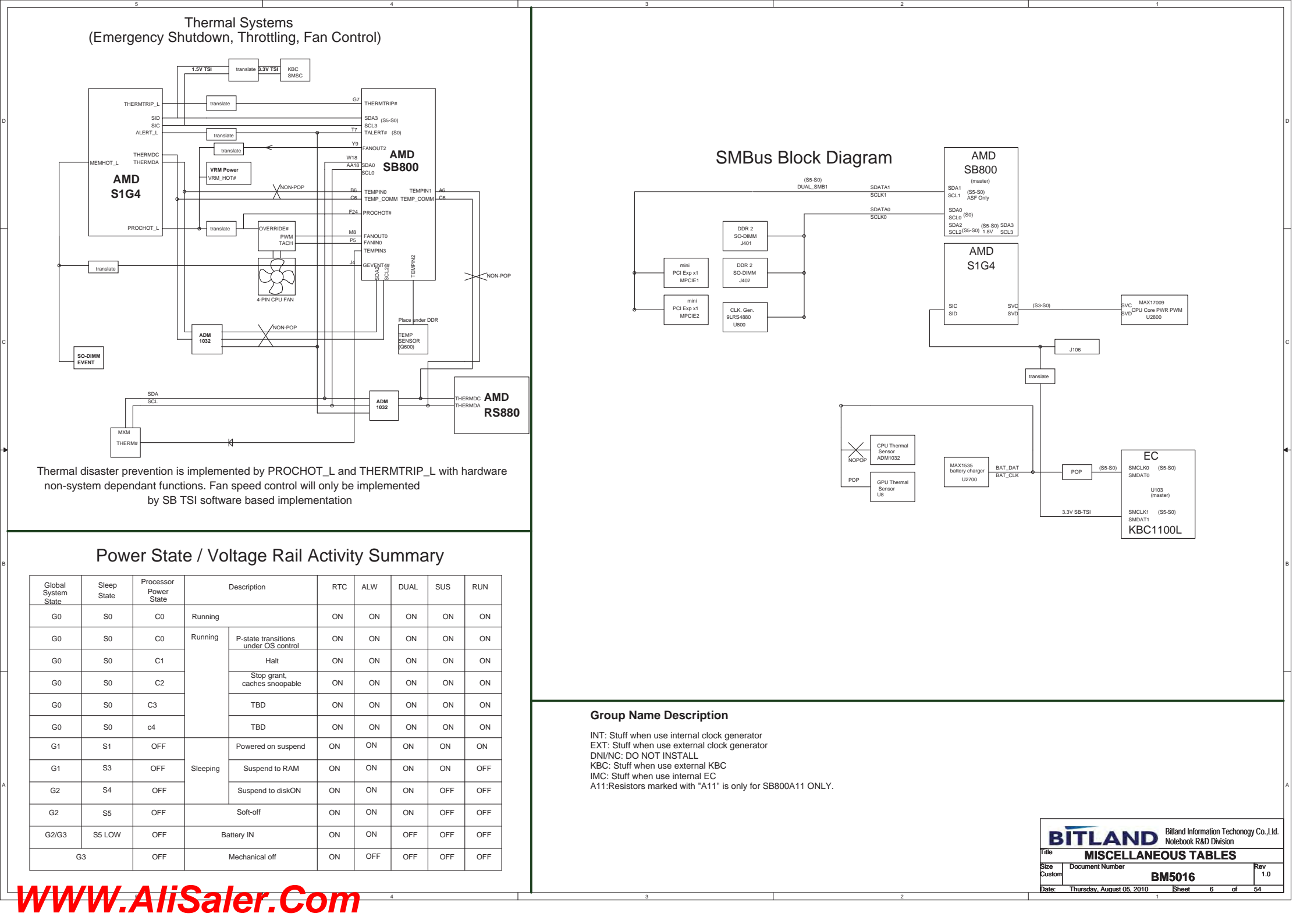


## EXTERNAL CLOCK MODE



## INTERNAL CLOCK MODE



[illegible][illegible][illegible][illegible]

**Thermal Systems**  
(Emergency Shutdown, Throttling, Fan Control)

Thermal disaster prevention is implemented by PROCOT\_L and THERMTRIP\_L with hardware non-system dependant functions. Fan speed control will only be implemented by SB TSI software based implementation

### SMBus Block Diagram

Global System State	Sleep State	Processor Power State	Description	RTC	ALW	DUAL	SUS	RUN
G0	S0	C0	Running	ON	ON	ON	ON	ON
G0	S0	C0	P-state transitions under OS control	ON	ON	ON	ON	ON
G0	S0	C1	Halt	ON	ON	ON	ON	ON
G0	S0	C2	Stop grant, caches snooperable	ON	ON	ON	ON	ON
G0	S0	C3	TBD	ON	ON	ON	ON	ON
G0	S0	c4	TBD	ON	ON	ON	ON	ON
G1	S1	OFF	Powered on suspend	ON	ON	ON	ON	ON
G1	S3	OFF	Suspend to RAM	ON	ON	ON	ON	OFF
G2	S4	OFF	Suspend to disk	ON	ON	ON	OFF	OFF
G2	S5	OFF	Soft-off	ON	ON	ON	OFF	OFF
G2/G3	S5 LOW	OFF	Battery IN	ON	ON	OFF	OFF	OFF
G3		OFF	Mechanical off	ON	OFF	OFF	OFF	OFF

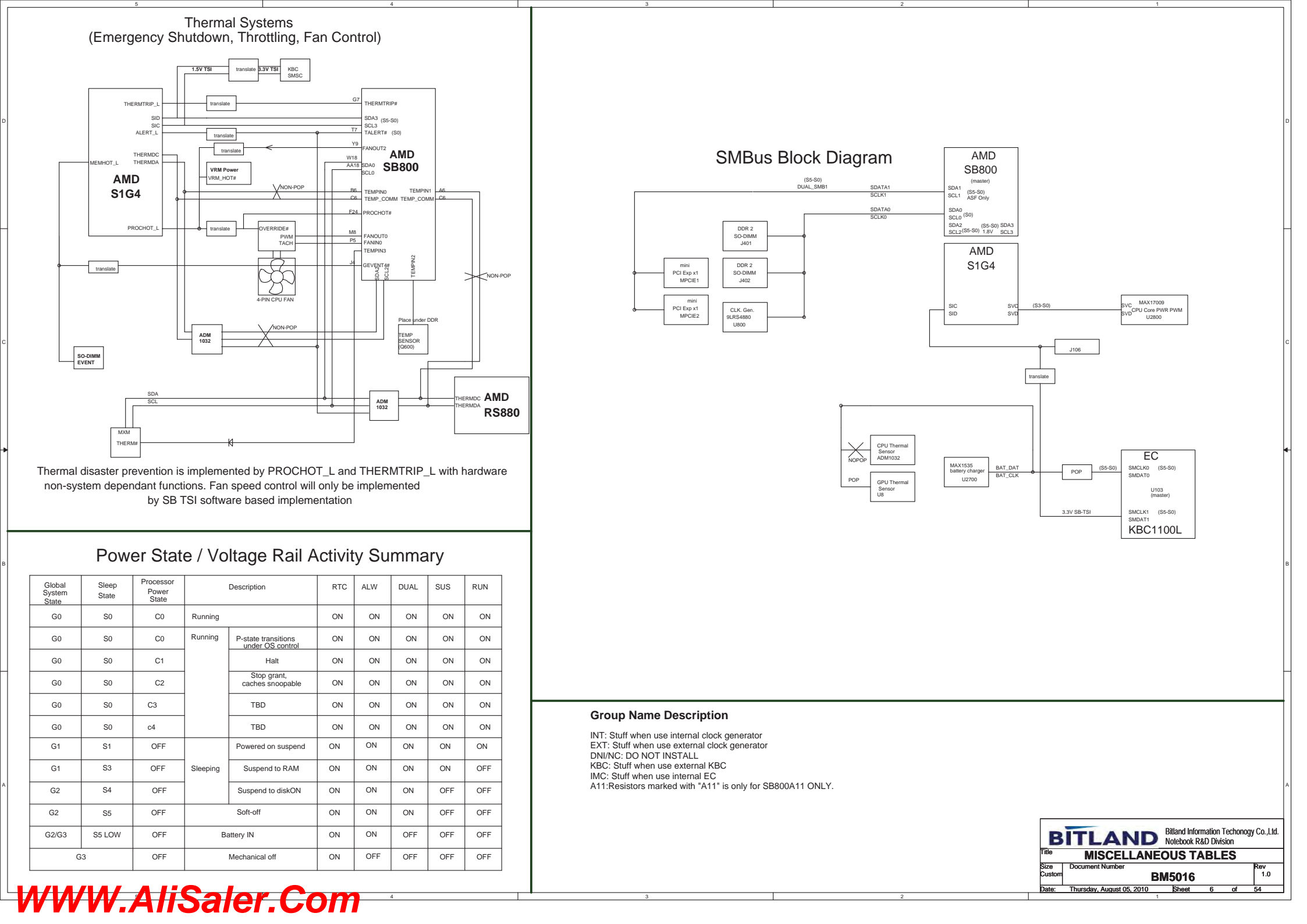
### Power State / Voltage Rail Activity Summary

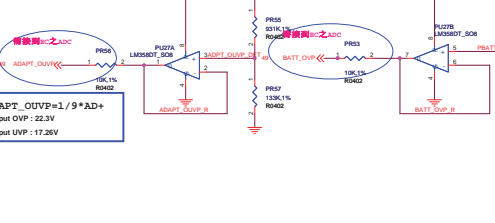
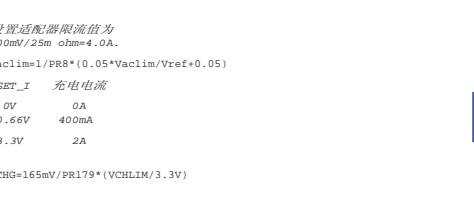
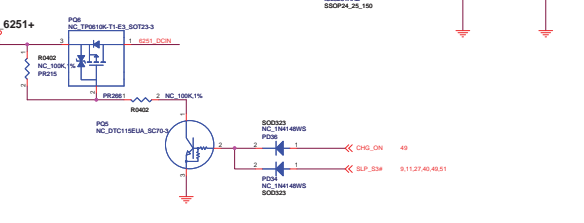
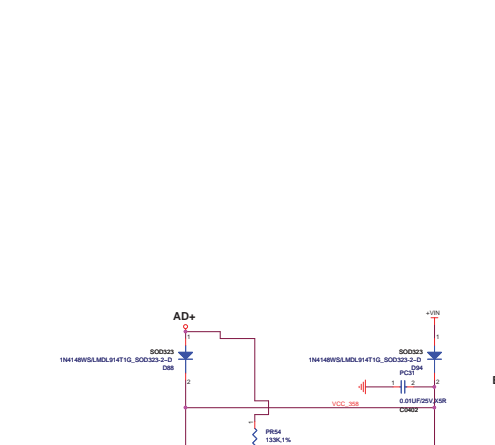
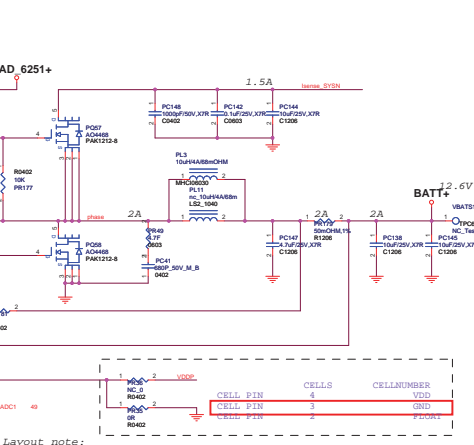
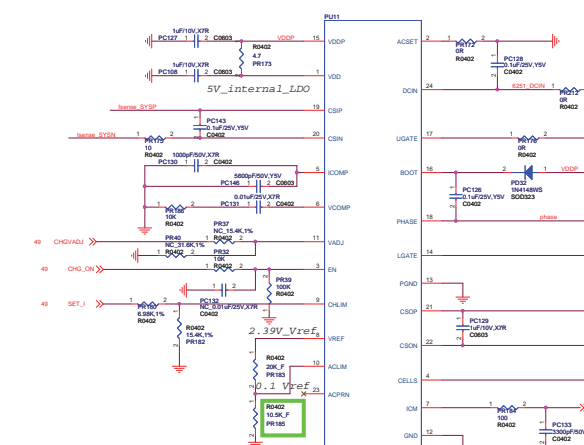
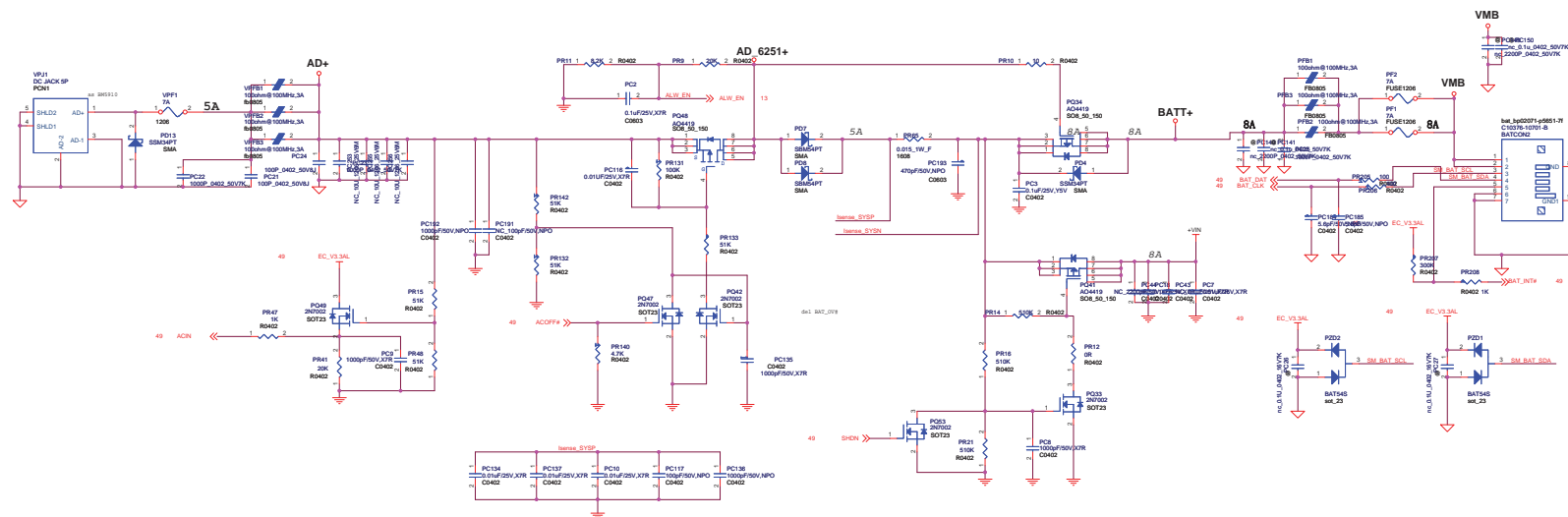
**Group Name Description**

- INT: Stuff when use internal clock generator
- EXT: Stuff when use external clock generator
- DNI/NC: DO NOT INSTALL
- KBC: Stuff when use external KBC
- IMC: Stuff when use internal EC
- A11: Resistors marked with "A11" is only for SB800A11 ONLY.

**BITLAND**  
 Bitland Information Technology Co., Ltd.  
 Notebook R&D Division  
**MISCELLANEOUS TABLES**  
 Title: BM5016  
 Size Custom Document Number Rev 1.0  
 Date: Thursday, August 05, 2010 Sheet 6 of 54

[illegible]



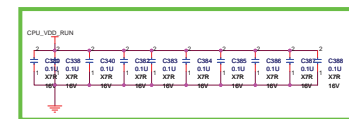
Layout note:  
Far away from critical signal trace

设置适配器限流值为  
100mA/25m ohm=4.0A.  
 $I_{ACLIM} = I_{PR8} * (0.05 * V_{ACIM} / V_{REF} + 0.05)$   
SET\_I 充电电流  
0V 0A  
0.66V 400mA  
3.3V 2A  
 $ICHG = 165mV / PR179 * (V_{CHLIM} / 3.3V)$

有誤用之ADC  
ADAPT\_OUVP=1/9\*AD+  
Input OVP: 22.3V  
Input UVP: 17.25V

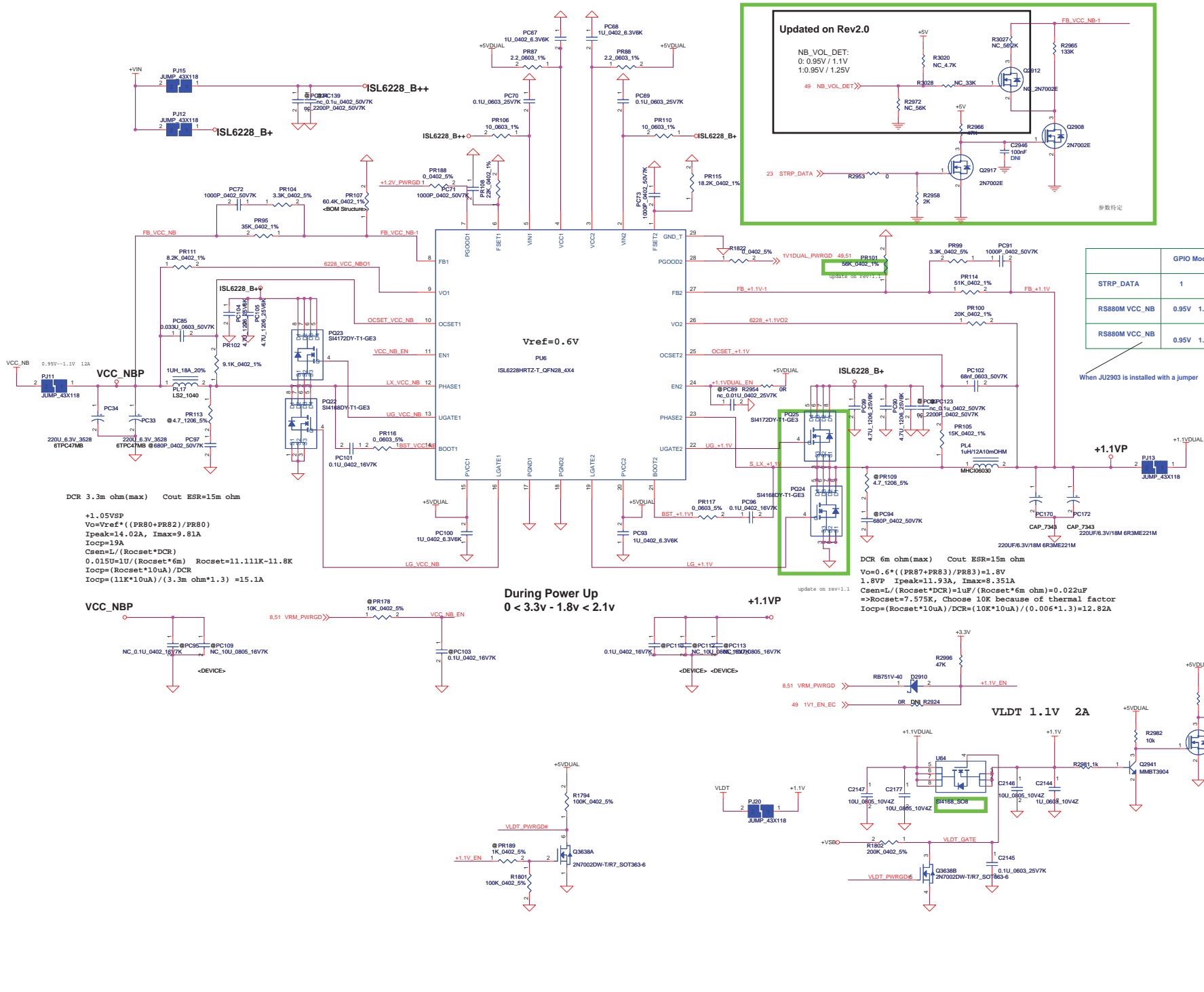
BATT\_OVP=1/9\*BATT+  
L2-4CELLS: 13.9V---BATT\_OVP=1.5012V  
L2-6CELLS: 18.0V---BATT\_OVP=2.0012V

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

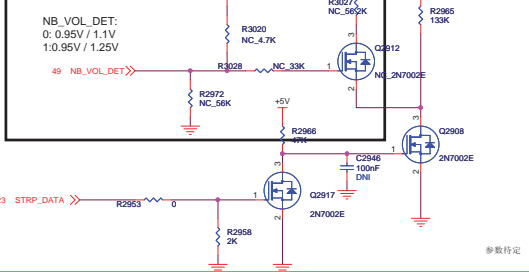








Updated on Rev2.0

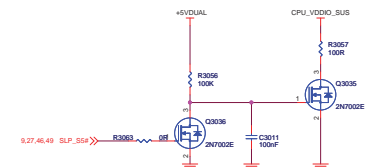
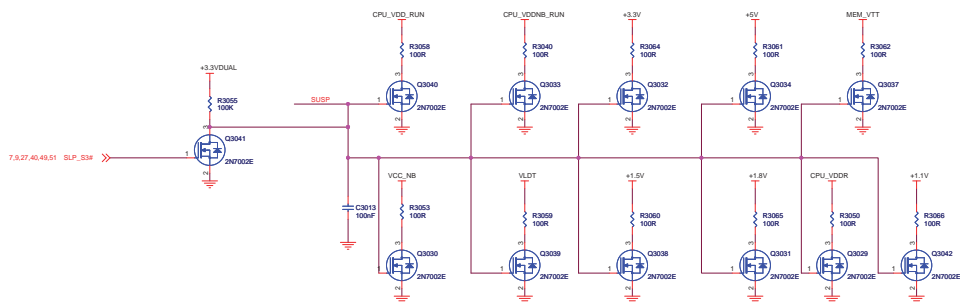
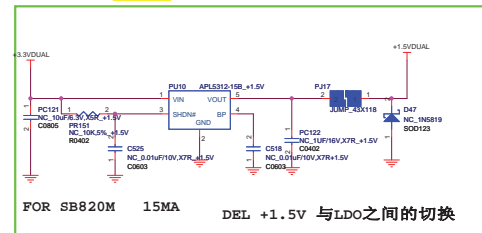
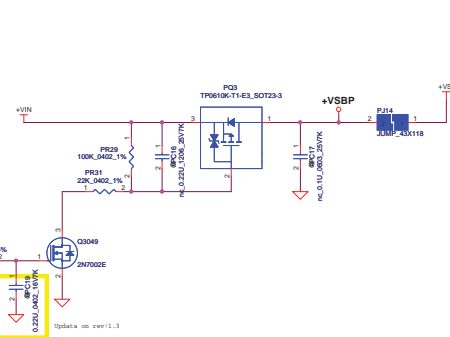
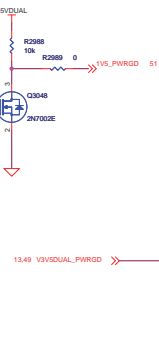
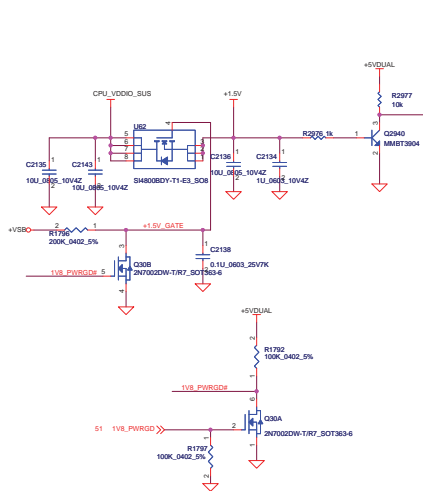
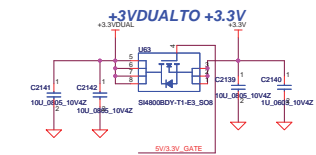
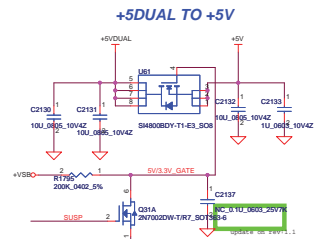
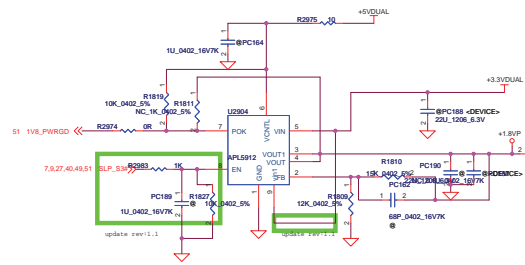


	GPIO Mode	Power Shift
STRP_DATA	1 0	PWM
RS880M VCC_NB	0.95V 1.1V	N/A
RS880M VCC_NB	0.95V 1.25V	

When JU2903 is installed with a jumper

During Power Up  
0 < 3.3V - 1.8V < 2.1V

DCR 6m ohm(max) Cout ESR=15m ohm  
Vo=0.6\*((PR87+PR83)/PR83)=1.8V  
1.8VP Ipeak=11.93A, Imax=8.351A  
Csen=L/(Rocset\*DCR)=1uF/(Rocset\*6m ohm)=0.022uF  
=>Rocset=7.575K, Choose 10K because of thermal factor  
Iocp=(Rocset\*10uA)/DCR=(10K\*10uA)/(0.006\*1.3)=12.82A



5

4

3

2

1

D

D

C

C

B

B

A

A

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<b>BITLAND</b>		Billand Information Technology Co.,Ltd. Notebook R&D Division	
Title		//	
Size	Document Number	Rev	
C	BM5016	1.0	
Date:	Thursday, August 05, 2010	Sheet	12 of 54

Iocp=10.8A

参数设定: Vo1=5.01V ;Vo2=3.3V

Update on rev1.1.1

NOTE: H--> 5v  
L--> 4.65V

ADD RESISTOR TO GET -5% LOWER FOR +3.3V(3.1626V)

改变PR24取值, EN V3AL的网络号

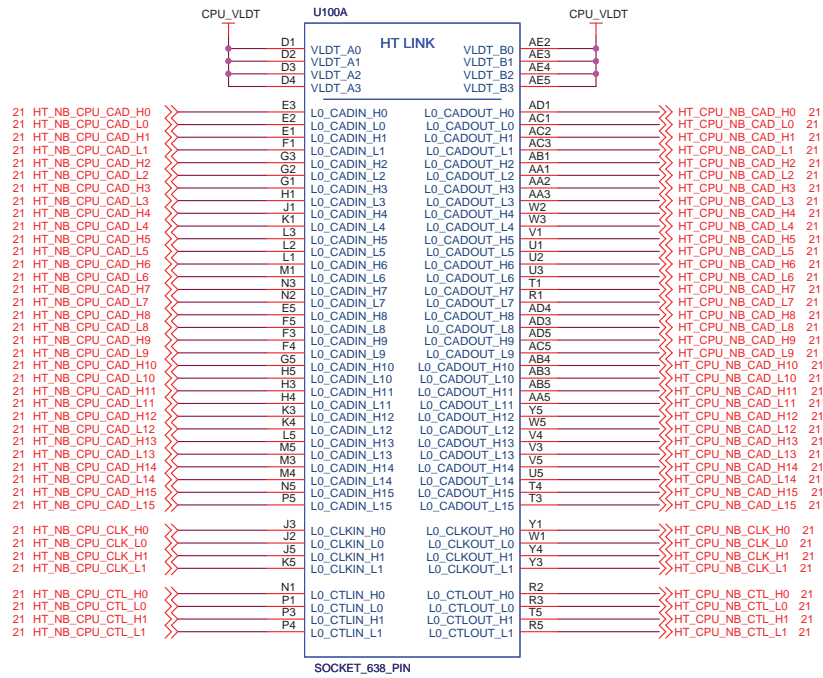
改变PR25取值, EN V5AL的网络号

Iocp=9.7A

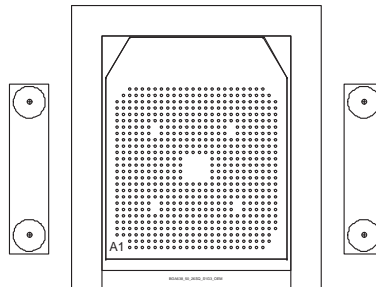
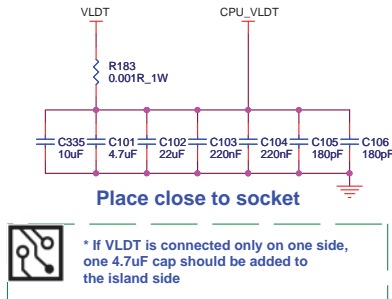
Add Enable/OCP Circuit 090918


BITLAND				Billand Information Technology Co.,Ltd.	
SYSTEM PWR				Notebook R&D Division	
Title	Document Number			Rev	
Size	BM5016			1.0	
Date:	Thursday, August 05, 2010			Sheet	13 of 54

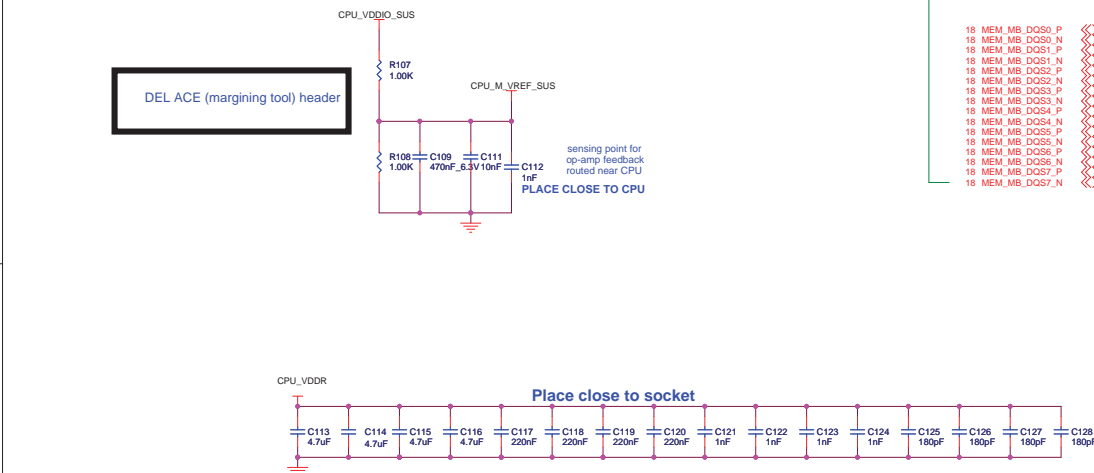
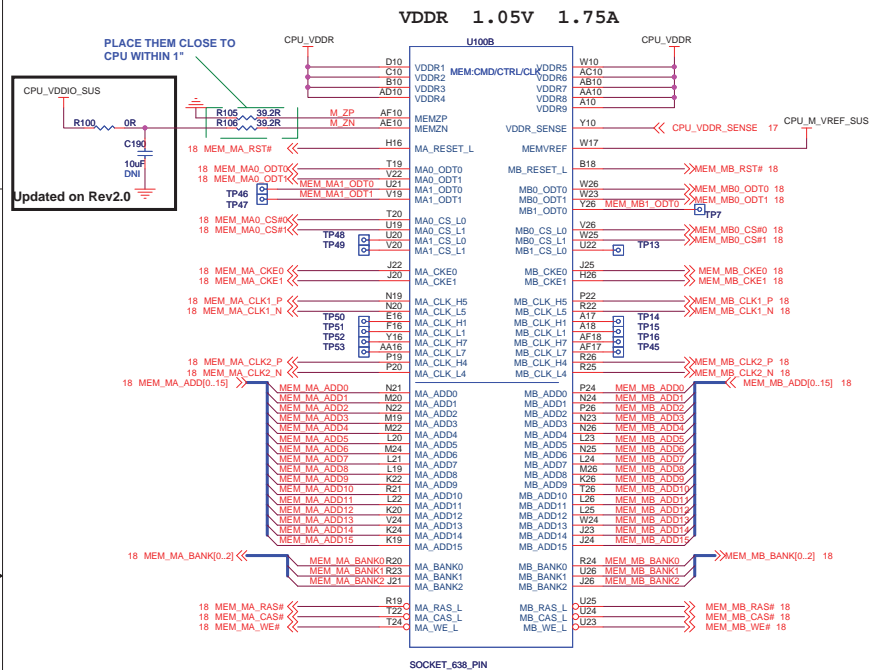
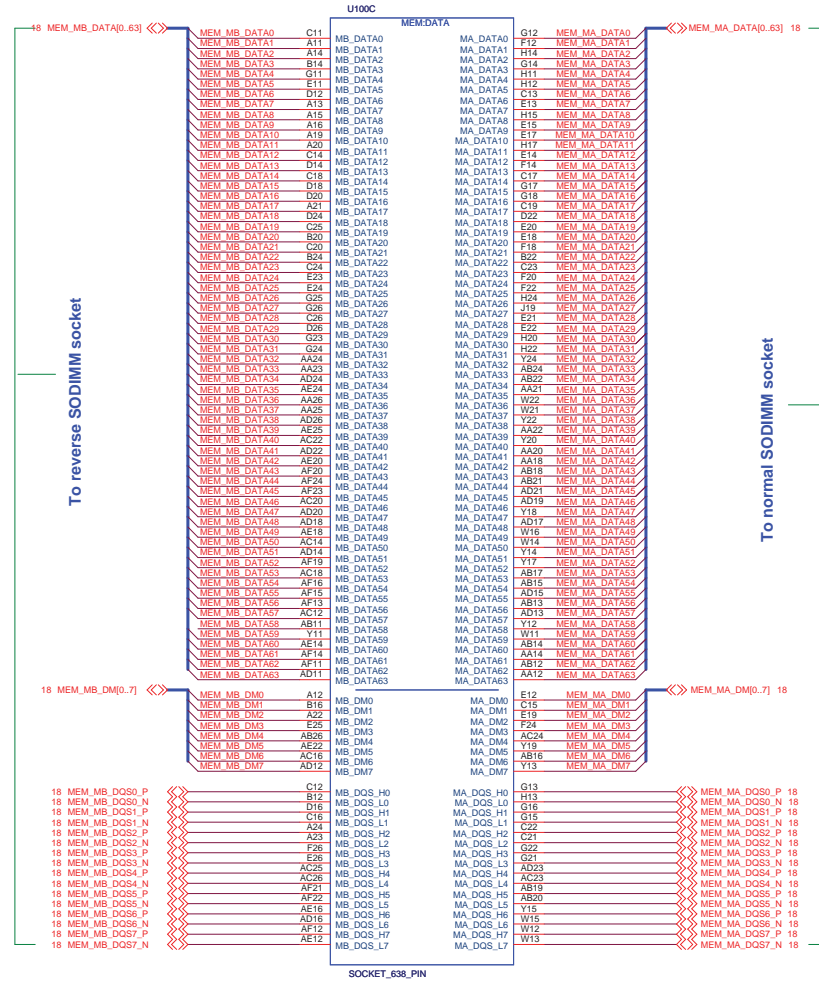
# CPU\_VLDT 1.1V 1.5A



DEL HTPA Soft-Touch Duo Connectors



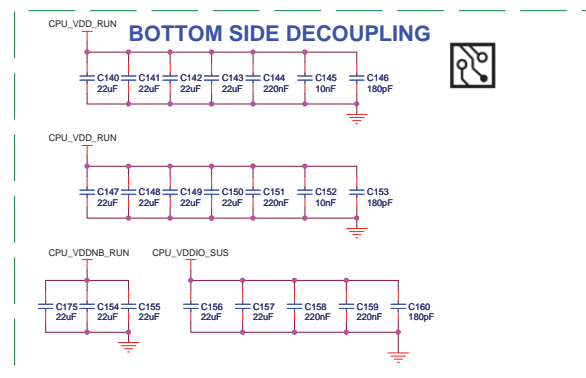
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Title <b>S1G4 HT V/F</b>			
Size Custom	Document Number <b>BM5016</b>		Rev 1.0
Date:	Thursday, August 05, 2010	Sheet	14 of 54



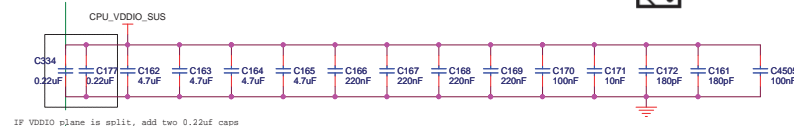




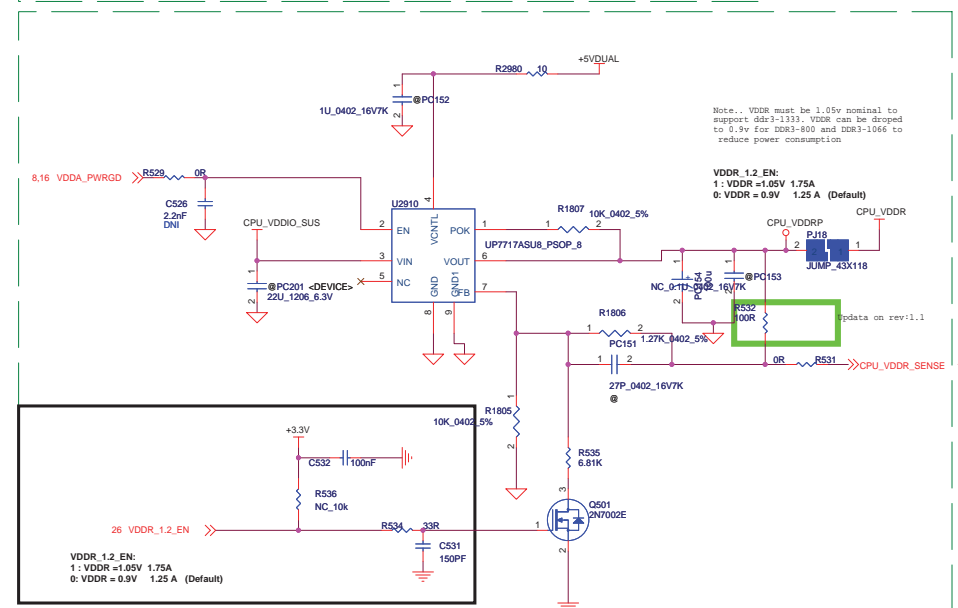
```
cpu_vddio_sus 3A
```



**DECOUPLING BETWEEN PROCESSOR AND DIMMs**  
**PLACE CLOSE TO PROCESSOR AS POSSIBLE**



IF VDDIO plane is split, add two 0.22uf cap

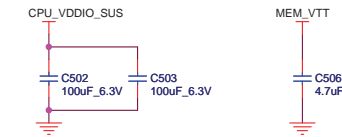
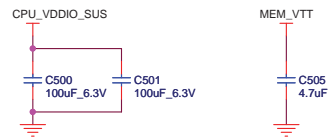
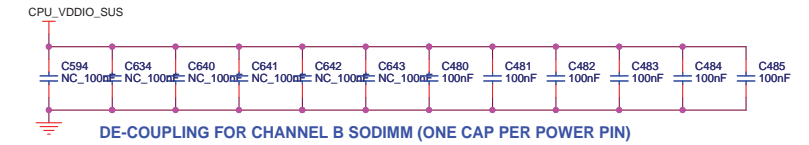
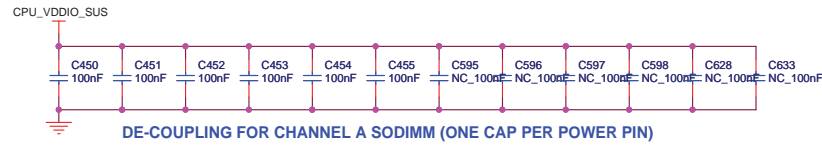
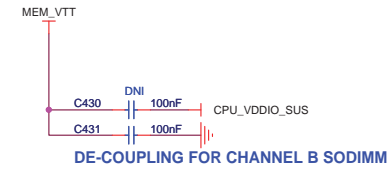
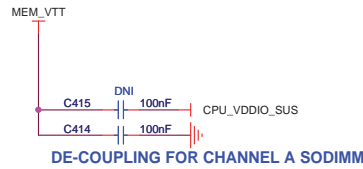


Note.. VDDR must be 1.05v nominal to support ddr3-1333. VDDR can be dropped to 0.9v for DDR3-800 and DDR3-1066 to reduce power consumption

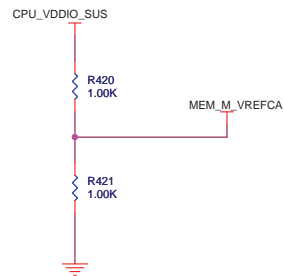
VDDR\_1.2\_EN:  
1 : VDDR = 1.05V 1.75A  
0: VDDR = 0.9V 1.25 A (Default)

Update on rev:1.

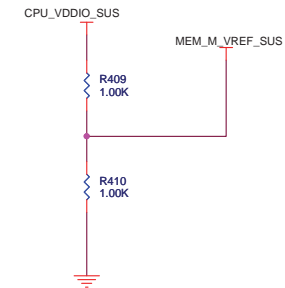




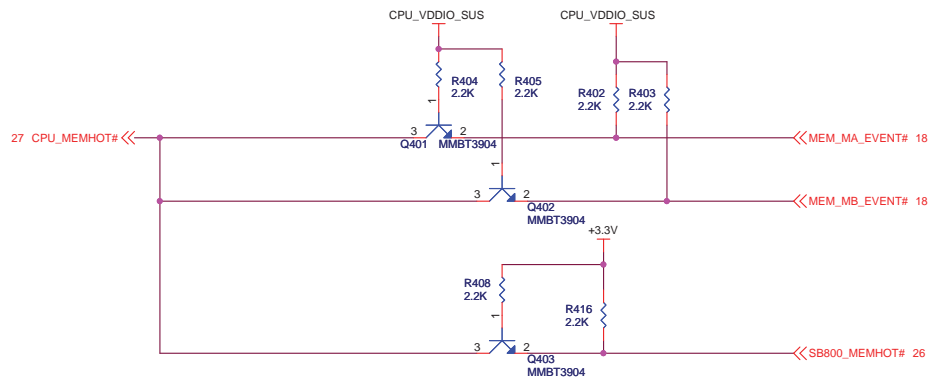
 LAYOUT: PLACE CLOSE TO DIMMs




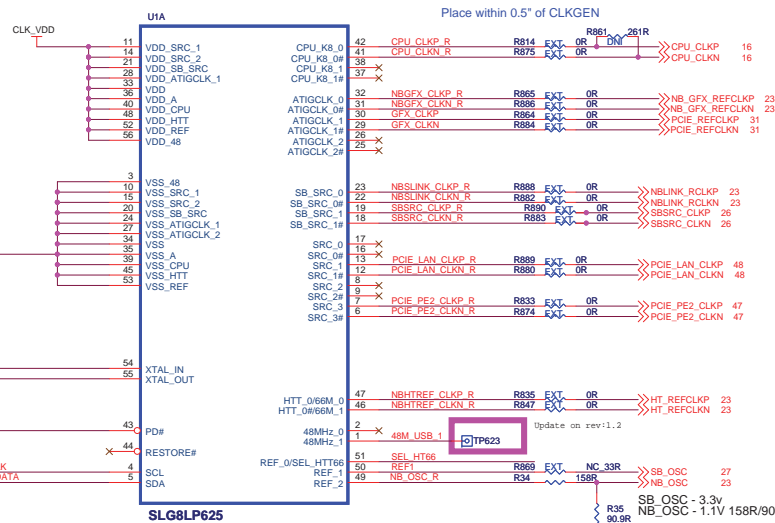
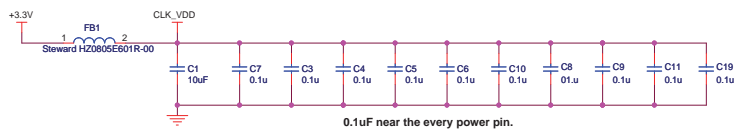
## MEM\_VREF\_SUS



 LAYOUT: PLACE CLOSE TO DIMMs



		Bitland Information Technology Co., Ltd.	
		Notebook R&D Division	
Title		<b>DDR3 SODIMM DECOUPLING</b>	
Size	Document Number	<b>BM5016</b>	Rev 1.0
Custom			
Date:	Thursday, August 05, 2010	Sheet	19 of 54



Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	6M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

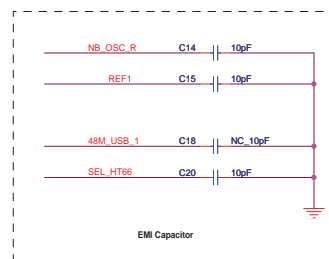
\* RS780 can be used as clock buffer to output two PCIe reference clocks. By default, chip will configured as input mode, BIOS can program it to output mode.

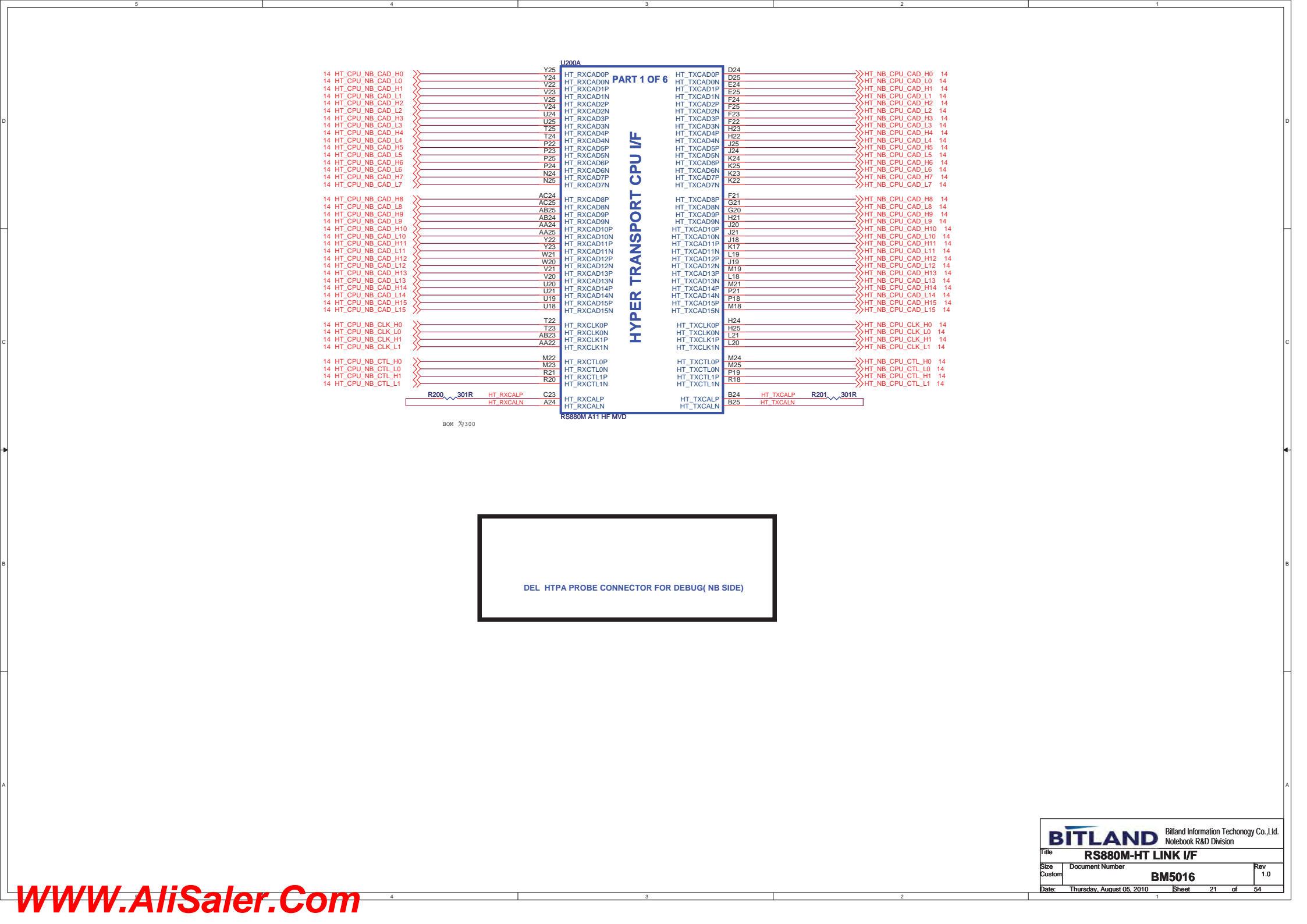
R34/R35 (value may change)

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 33R/43R
RS780	1.1V 200R/100R

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock

\* default



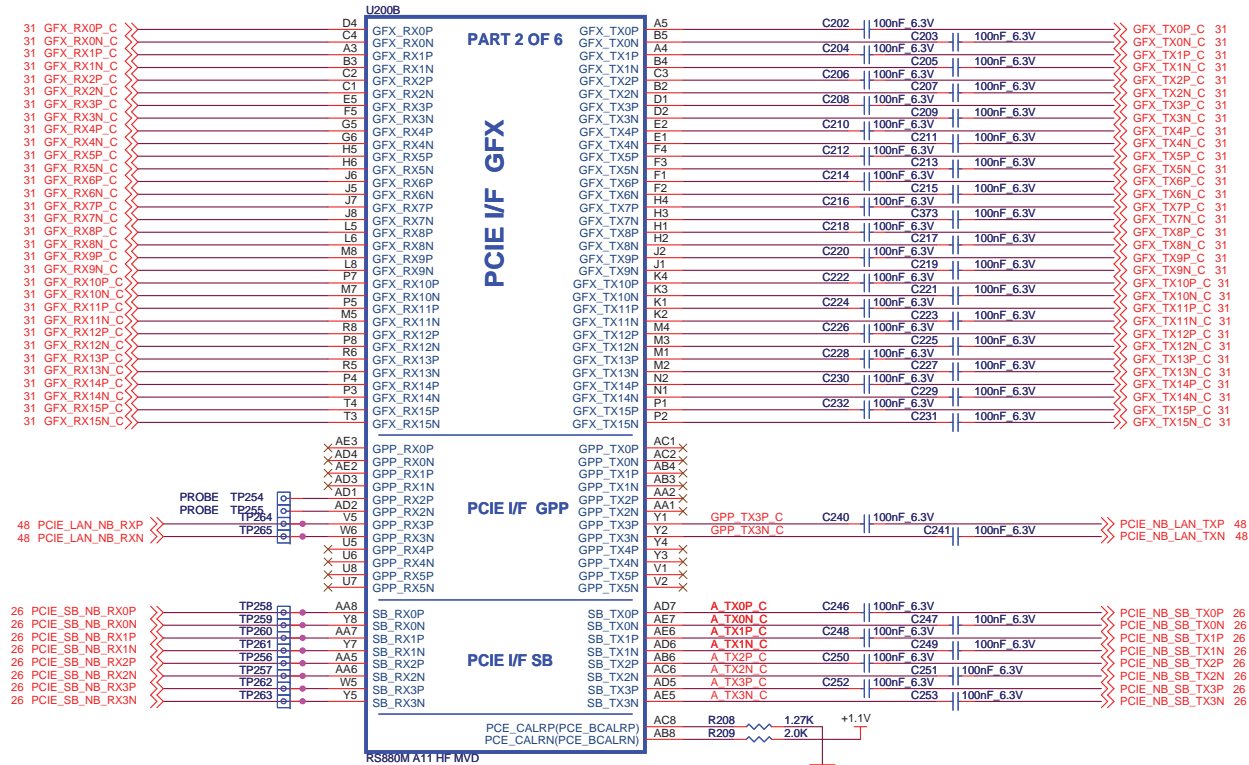




MXM3.0 need put the CAP on the motherboard.  
Close to the MXM Slot



MXM3.0 need put the CAP on the motherboard.  
Close to the MXM Slot

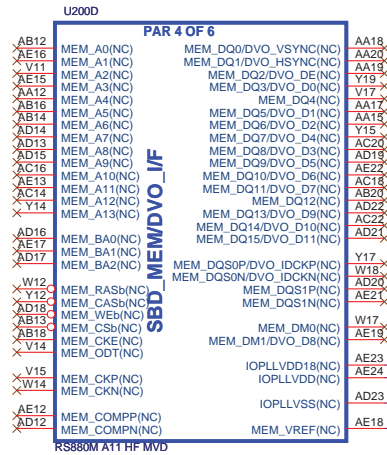


Keep the impedance of PCIE lane to 85ohm +/-15%  
Including the A-link



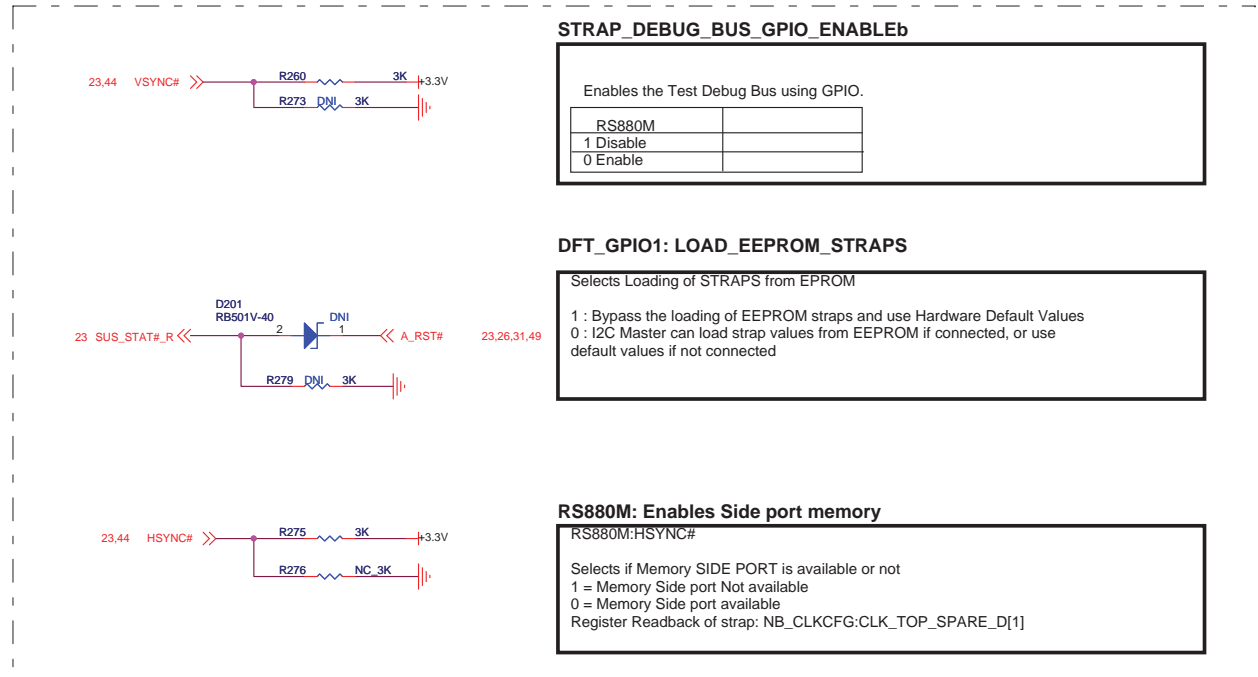
All PCIE lane shou route 8" max for Gen2 connector and max 12" for Gen2 on board devices  
Guam has the Lasso lane over 8" due to the large board, should use shorter lasso calbe for Guam.  
Customer need to follow the MBDG.



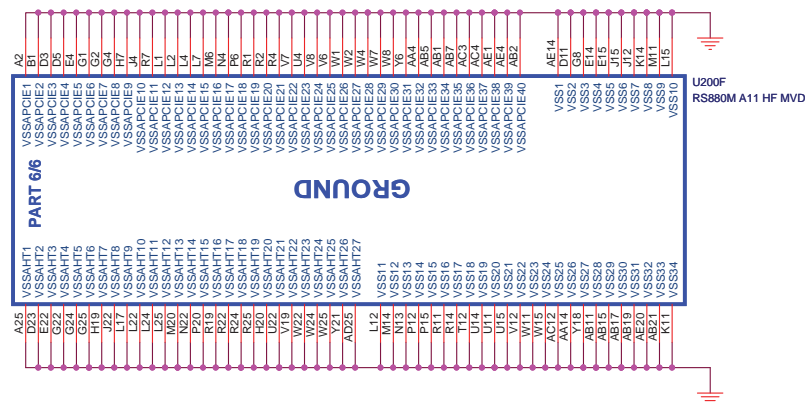


DEL U202

DEL SDRAM DDR3

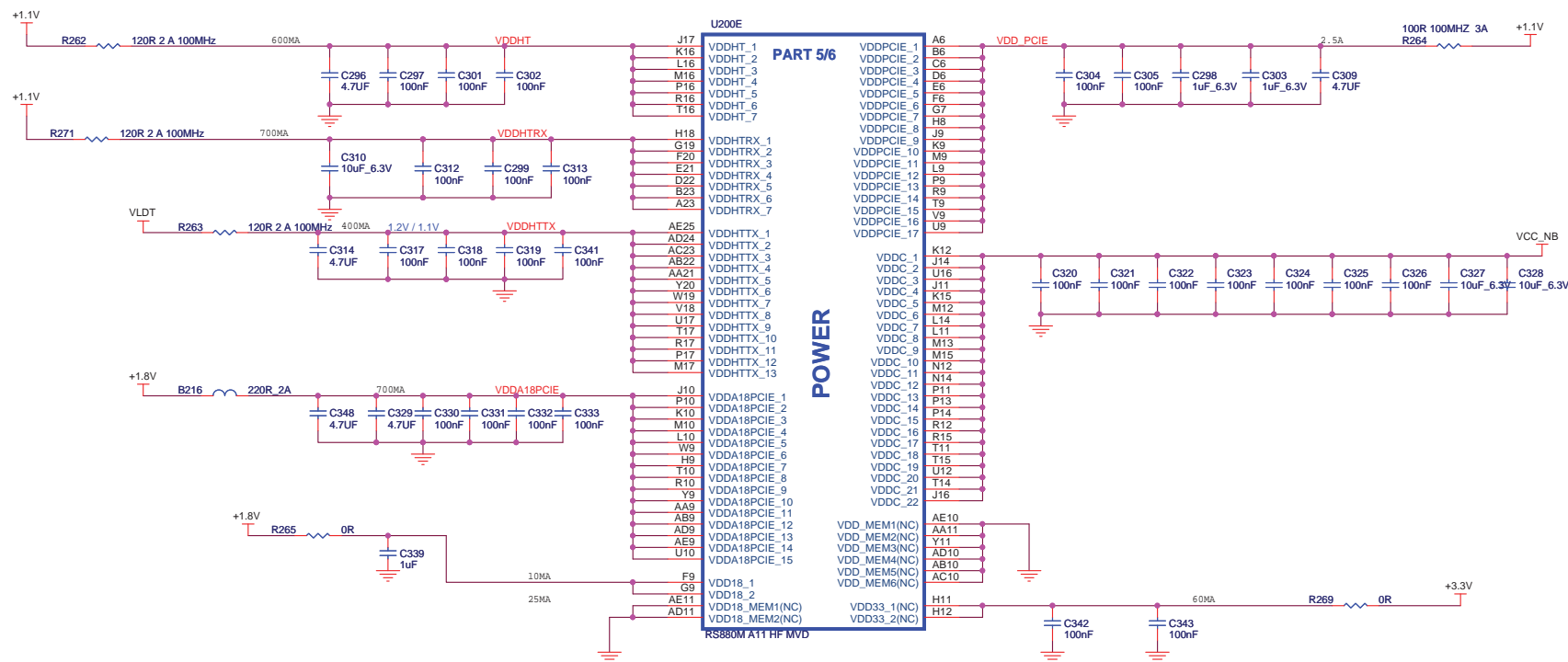






RS880M POWER TABLE

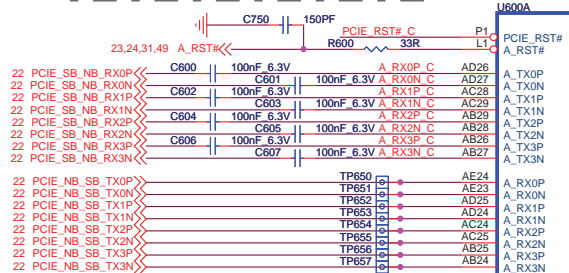
PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVD18	+1.8V	VDDL33	NC



DEL FAN CIRCUIT

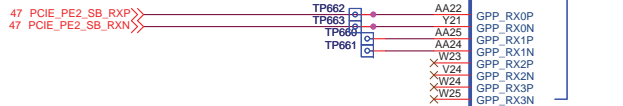


PLACE THESE PCIE AC  
COUPLING CAPS CLOSE TO U600



J613 CLOSE TO U600

NOTE: SB8XX ONLY SUPPORTS 2 GPP  
PORT 2 AND 3 IS NOT SUPPORTED.



NOTE: The 0R serial resistor on SB CLK pair  
must share Pad with the serial resistor close to U600

FOR EXT GRAPHICS

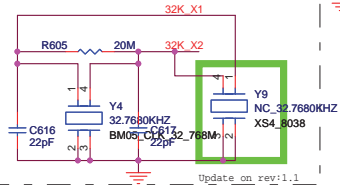
FOR WIFI

FOR LAN

Updated on Rev2.0

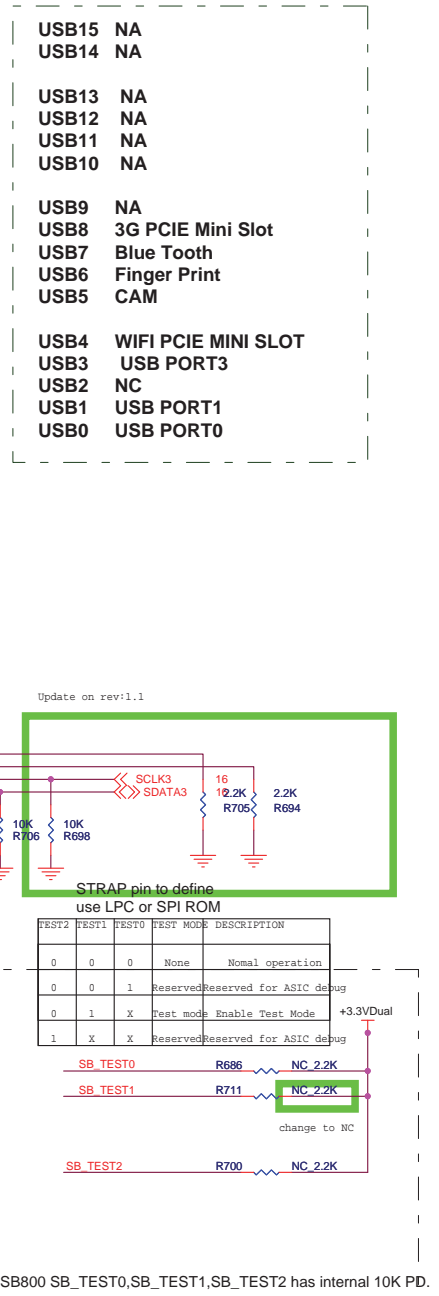
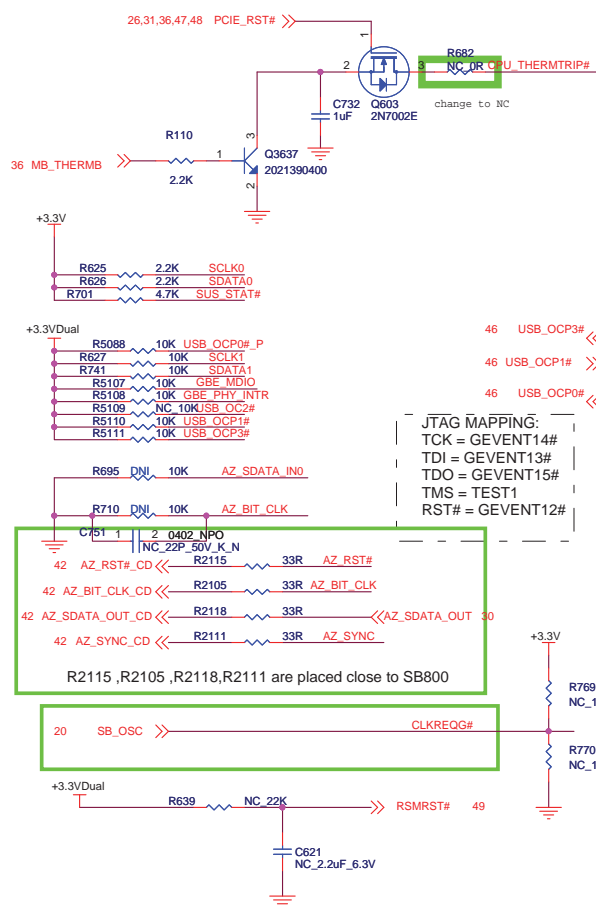


PLACE THESE COMPONENTS CLOSE TO U600, AND  
USE GROUND GUARD FOR 32K\_X1 AND 32K\_X2



Update on rev:1.1





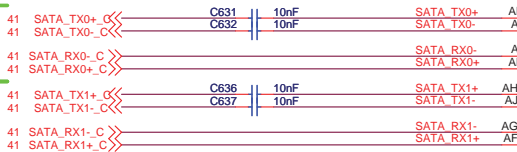
TEST2	TEST1	TEST0	TEST MODE	DESCRIPTION
0	0	0	None	Normal operation
0	0	1	Reserved	Reserved for ASIC debug
0	1	X	Test mode	Enable Test Mode
1	X	X	Reserved	Reserved for ASIC debug

SB800 SB TEST0.SB TEST1.SB TEST2 has internal 10K PD.



SATA trace should use only 1via on the trace. customers can use 2vias with GND via within 150mils of signal via as long as they can ensure that their platform meets SATA logo requirements. Return loss is expected to get affected with 2 vias. AMD platforms are validated with one via only

FOR SATA HD



FOR SATA ODD

SATA PORTS DISTRIBUTION:

- 0, - 2.5 INCH DISK DRIVER
- 1, SATA, ODD
- 2, NOT USED
- 3, NOT USED
- 4 & 5, NOT USED



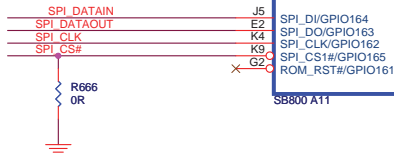
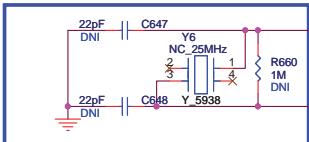
PLACE SATA\_CAL RES VERY CLOSE TO BALL OF U600



51

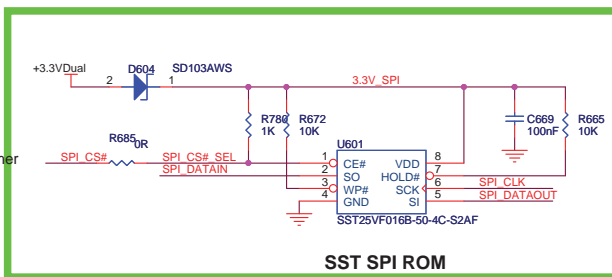
SATA\_ACT#

To meet SB800 SCL1.02:  
DNI SATA XTAL circuit's parts



R685: Normal

R666: EXT Programmer



change to SPI mode

SB800  
Part 2 of 5

SERIAL ATA

FLASH

HW MONITOR

SPI ROM

U600B

AH9

AJ9

AH8

AH10

AJ10

AG10

AF10

AG12

AF12

AH12

AH12

AH14

AJ14

AG14

AF14

AG17

AF17

AJ17

AH17

AJ18

AH18

AH19

AJ19

AB14

AA14

AD11

AD16

AC16

J5

E2

K4

K9

G2

NC1

NC2

SB800 A11

SATA\_TX0P

SATA\_TX0N

SATA\_RX0N

SATA\_RX0P

SATA\_TX1P

SATA\_TX1N

SATA\_RX1N

SATA\_RX1P

SATA\_TX2P

SATA\_TX2N

SATA\_RX2N

SATA\_RX2P

SATA\_TX3P

SATA\_TX3N

SATA\_RX3N

SATA\_RX3P

SATA\_TX4P

SATA\_TX4N

SATA\_RX4N

SATA\_RX4P

SATA\_TX5P

SATA\_TX5N

SATA\_RX5N

SATA\_RX5P

FC\_CLK

FC\_FBCLKOUT

FC\_FBCLKIN

FC\_OE#/GPIO145

FC\_AVDD#/GPIO146

FC\_WE#/GPIO148

FC\_CE1#/GPIO149

FC\_CE2#/GPIO150

FC\_INT1/GPIO144

FC\_INT2/GPIO147

FC\_ADQ0/GPIO128

FC\_ADQ1/GPIO129

FC\_ADQ2/GPIO130

FC\_ADQ3/GPIO131

FC\_ADQ4/GPIO132

FC\_ADQ5/GPIO133

FC\_ADQ6/GPIO134

FC\_ADQ7/GPIO135

FC\_ADQ8/GPIO136

FC\_ADQ9/GPIO137

FC\_ADQ10/GPIO138

FC\_ADQ11/GPIO139

FC\_ADQ12/GPIO140

FC\_ADQ13/GPIO141

FC\_ADQ14/GPIO142

FC\_ADQ15/GPIO143

W5

W6

Y9

W7

V9

W8

B6

A6

A5

B5

C7

A3

B4

A4

C5

A7

B7

B8

A8

G27

Y2

TEMPIN0

TEMPIN1

TEMPIN2

TEMPIN3

TEMPIN4

TEMPIN5

TEMPIN6

TEMPIN7

TEMPIN8

TEMPIN9

TEMPIN10

TEMPIN11

TEMPIN12

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TEMPIN170

TEMPIN171

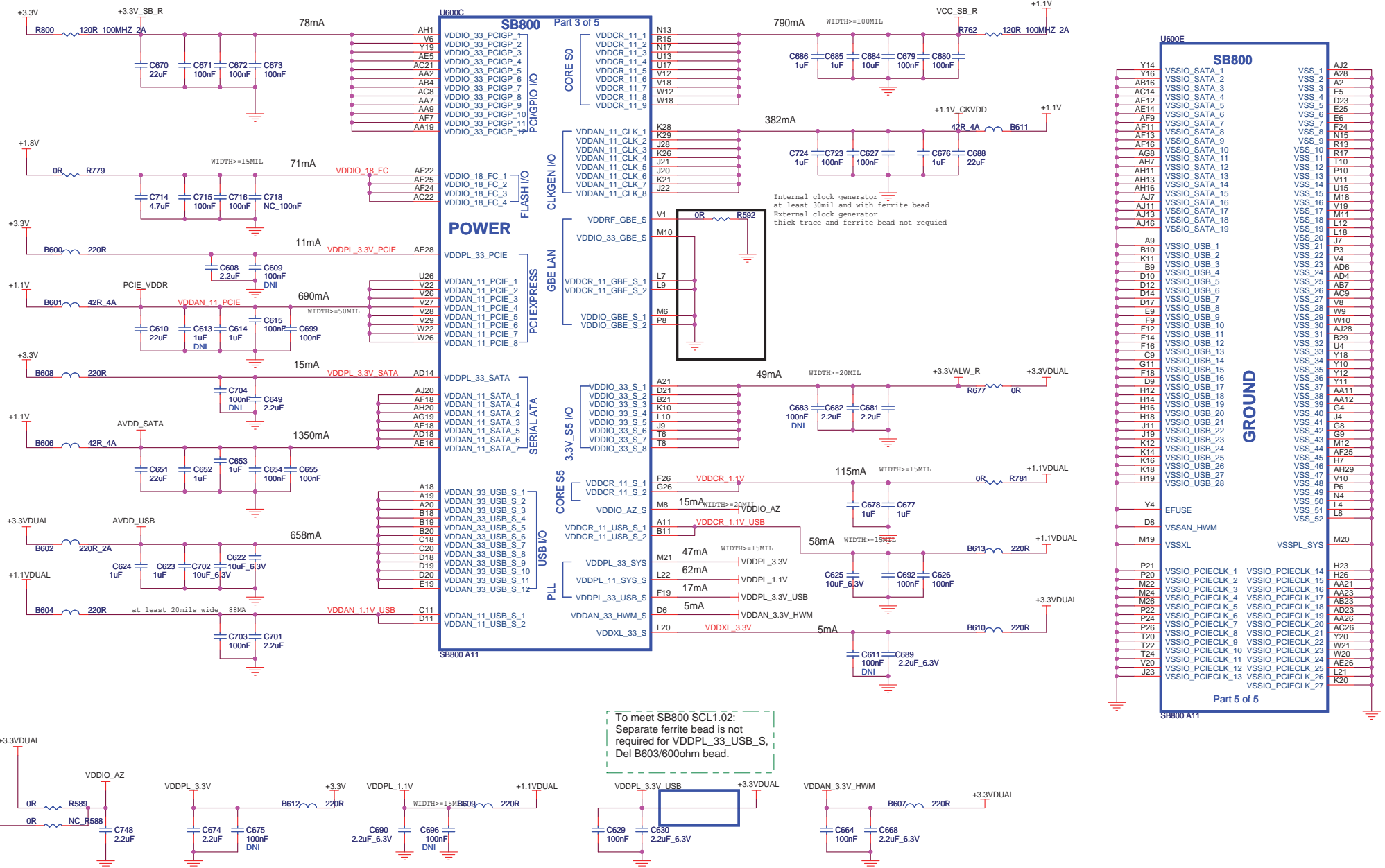
TEMPIN172

TEMPIN173

TEMPIN174

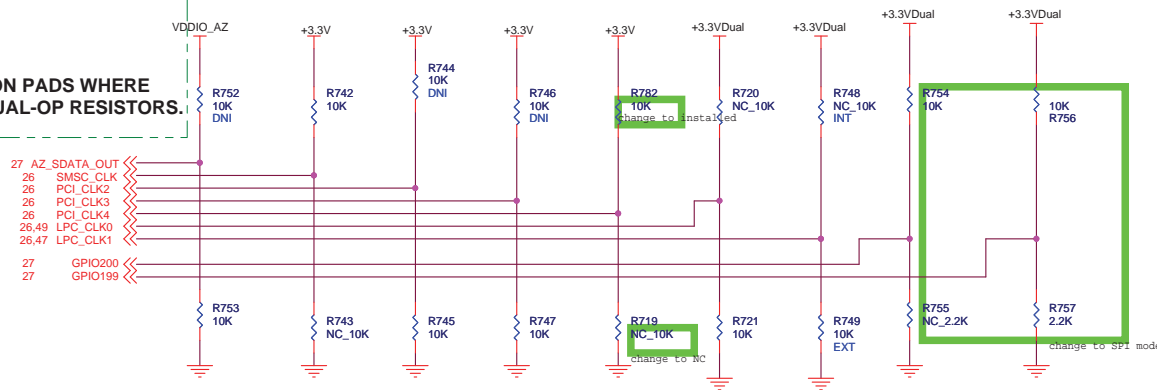


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.





OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



DEL JTAG HEADER

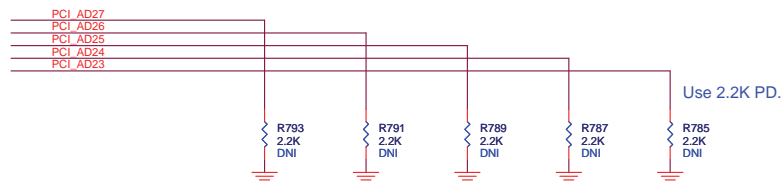
## REQUIRED STRAPS

	AZ_SDOUT	SMSC_CLK	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

## DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

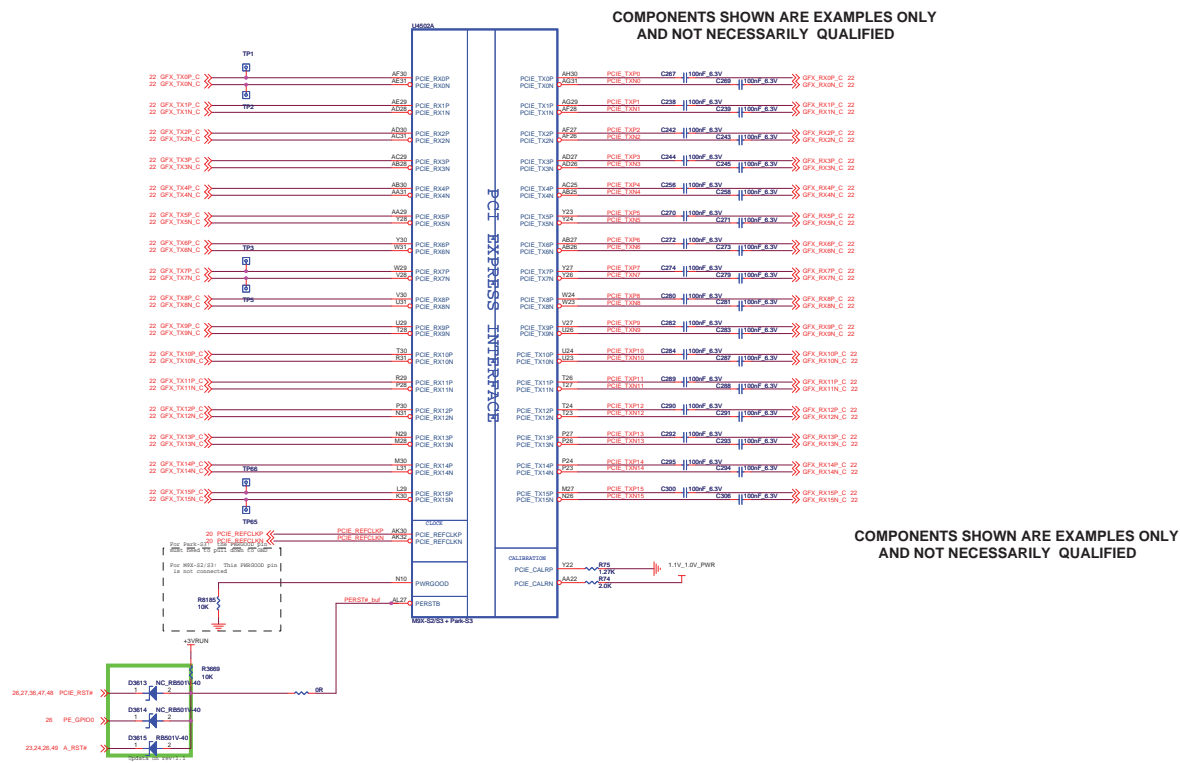
26 PCI\_AD[27..23] <<>>



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

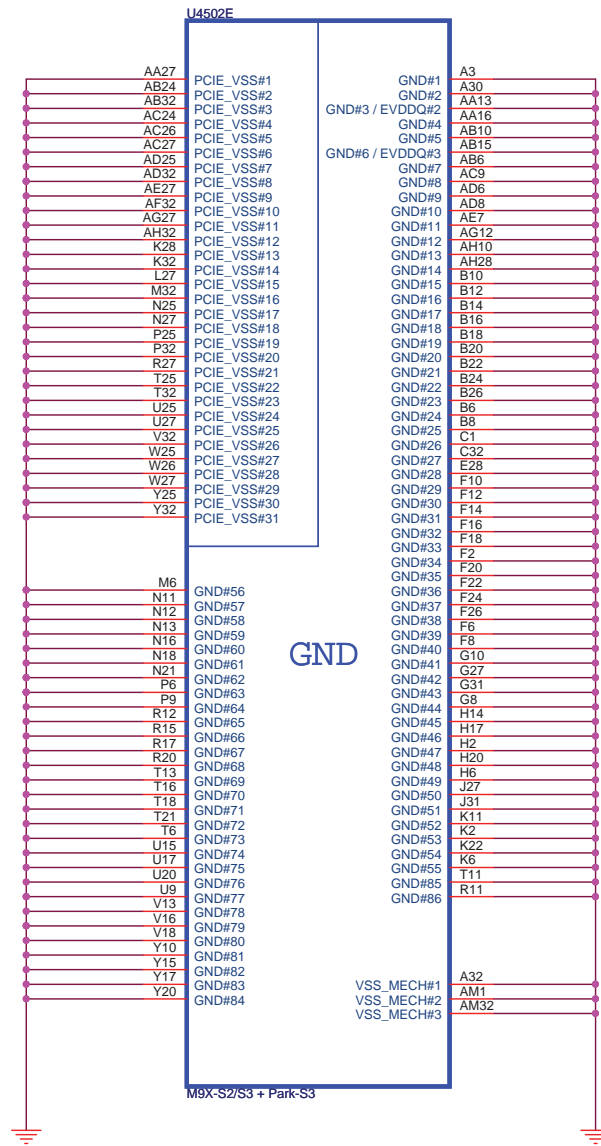
<b>BITLAND</b> Bitland Information Technology Co., Ltd. Notebook R&D Division	
Title <b>SB8X0-STRAPS</b>	
Size Custom	Document Number <b>BM5016</b>
Date: Thursday, August 05, 2010	Sheet 30 of 54




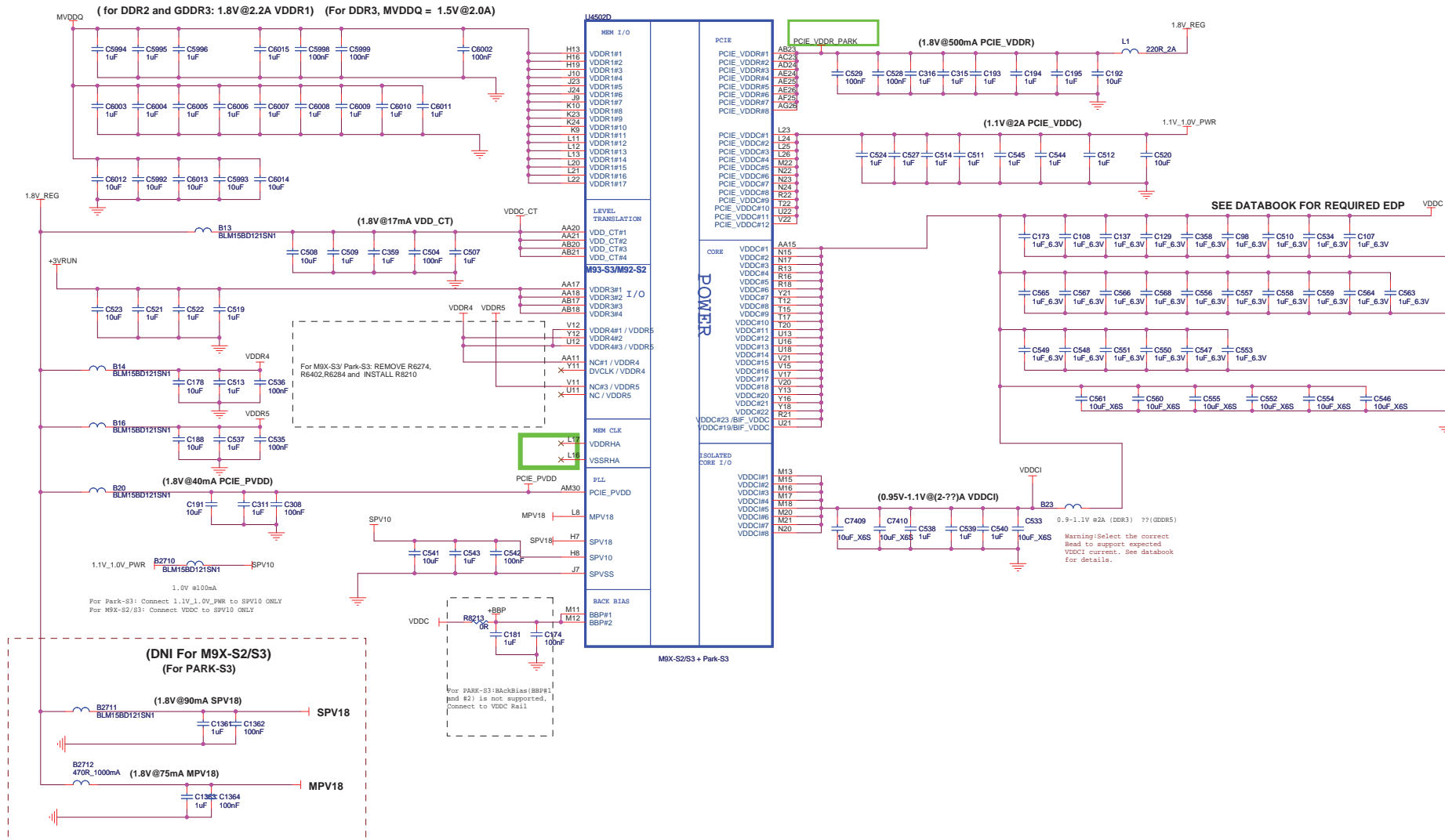


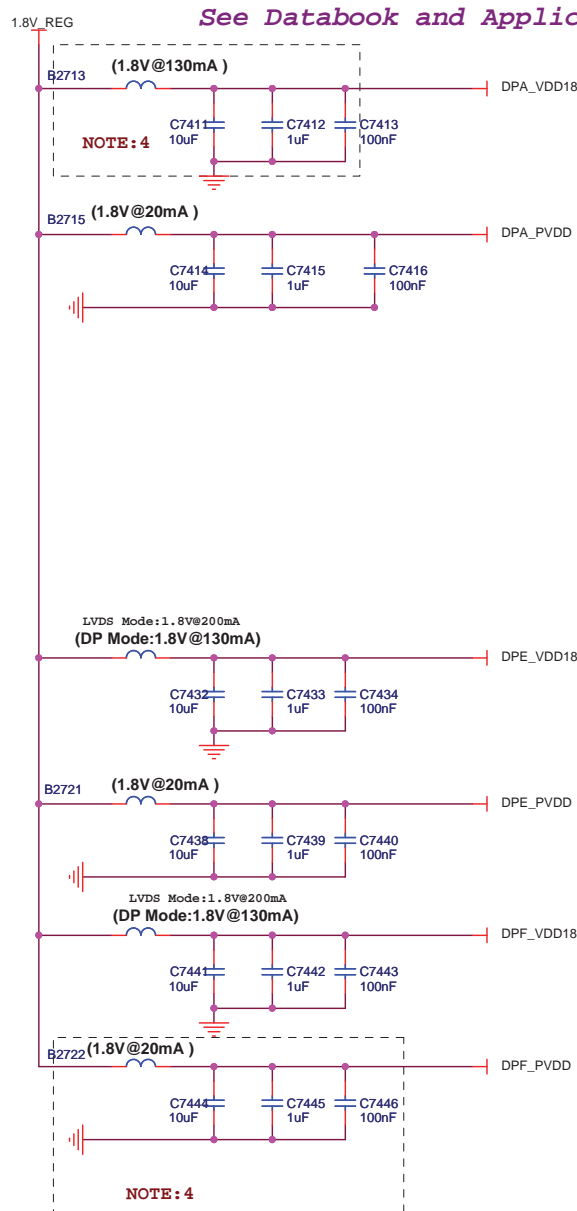






		Bitland Information Technology Co., Ltd. Notebook R&D Division	
Title <b>PARK-XT(Core_GND)</b>			
Size B	Document Number <b>BM5016</b>		Rev 1.0
Date:	Thursday, August 05, 2010	Sheet 33 of 54	

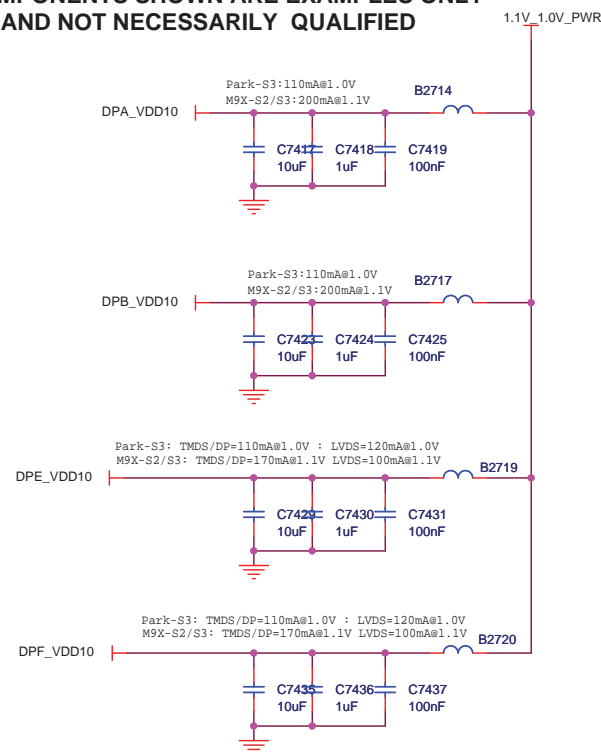
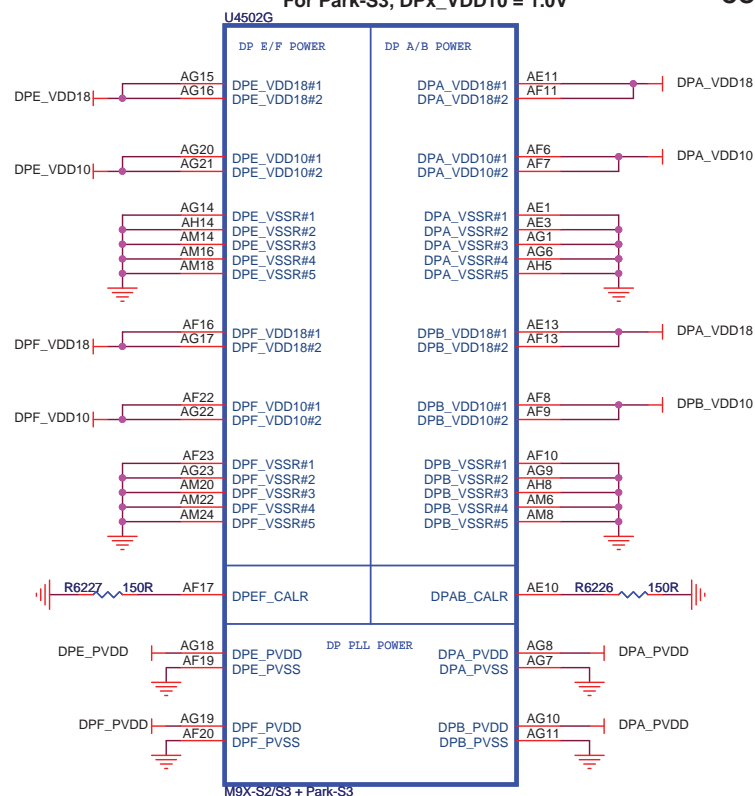




See Databook and Application note table for Voltage and Current requirements for each individual rail.

For M9X-S2/S3, DPx\_VDD10 = 1.1V  
For Park-S3, DPx\_VDD10 = 1.0V

COMPONENTS SHOWN ARE EXAMPLES ONLY  
AND NOT NECESSARILY QUALIFIED



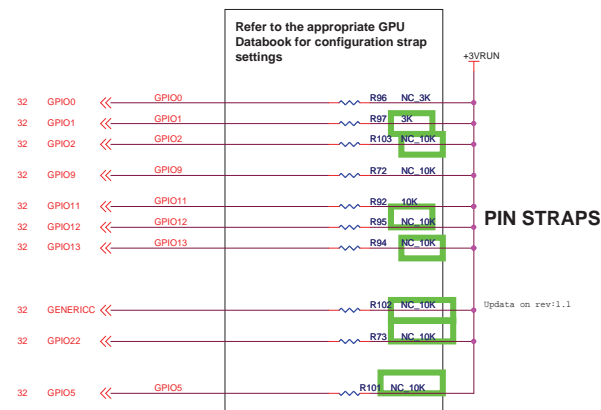
**NOTE:1:** DPx\_VDD18 and DPx\_PVDD Rails can be join together and remove Decoupling Capacitors and BEAD for DPx\_PVDD if signal integrity for DP lanes are OK.

**NOTE:2:** DPA\_VDD10 / DPB\_VDD10 and DPE\_VDD10 / DPF\_VDD10 Rails can be join together and remove Decoupling Capacitors and BEAD for one rail of each pair if signal integrity for DP lanes are OK. We also need to Change BEAD to minimum 400mA rating.

**NOTE:3:** DPx\_VDD18 Rails can be join together as shown in schematic for Dual -Link DVI or LVDS setting and remove Decoupling Capacitors and BEAD of any one rail of the pair if signal integrity for DP lanes are OK. We need atleast 500mA Bead to support join rails.

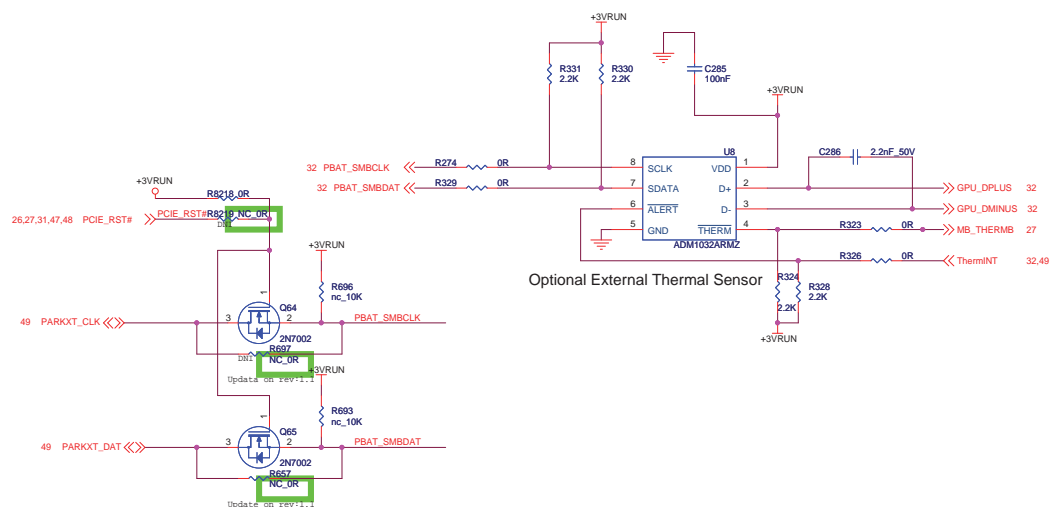
**NOTE:4:** Do not Install for M9X-S2/S3. INSTALL ONLY for PARK-S3. Other Notes can be apply as well.

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Title	<b>Park-XT(DP Power)</b>		
Size B	Document Number	<b>BM5016</b>	Rev 1.0
Date:	Thursday, August 05, 2010	Sheet 35 of 54	

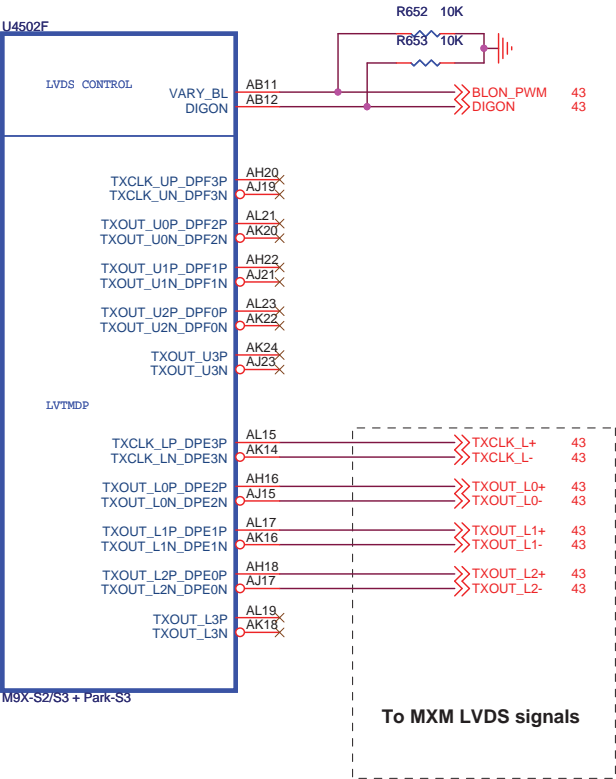



CONFIGURATION STRAPS			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X= DESIGN DEPENDANT NA= NOT APPLICABLE
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	X
RSVD	GPIO8	VGA ENABLED	0
BIF_VGA_DIS	GPIO9		0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD	GENERICC	AUD[1] AUD[0]	0
AUD[1]	HSYNC	0 0 No audio function	0
AUD[0]	VSXNC	0 1 Audio for DisplayPort and HDMI if dongle is detected	X X
		1 0 Audio for DisplayPort only	
		1 1 Audio for both DisplayPort and HDMI	

AMD RESERVED CONFIGURATION STRAPS	
H2SYNC	GENERICC
Provide pull-up pads for these straps - but do not populate. GPIOs functions on these signals must not conflict with the pin strap at Reset	
Provide pull-up pads for these straps - but do not populate. GPIOs functions on these signals must not conflict with the pin strap at Reset	
GPIO21_BB_EN	



LVDS Interface



		Bitland Information Technology Co., Ltd. Notebook R&D Division	
Title <b>Park-XT(DPEF_ LVDS)</b>			
Size B	Document Number <b>BM5016</b>		Rev 1.0
Date:	Thursday, August 05, 2010	Sheet 37 of 54	



PLACE MVREF DIVIDERS  
AND CAPS CLOSE TO ASIC

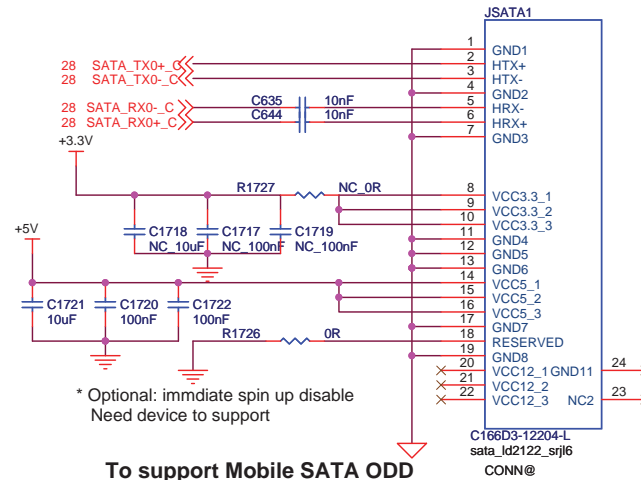




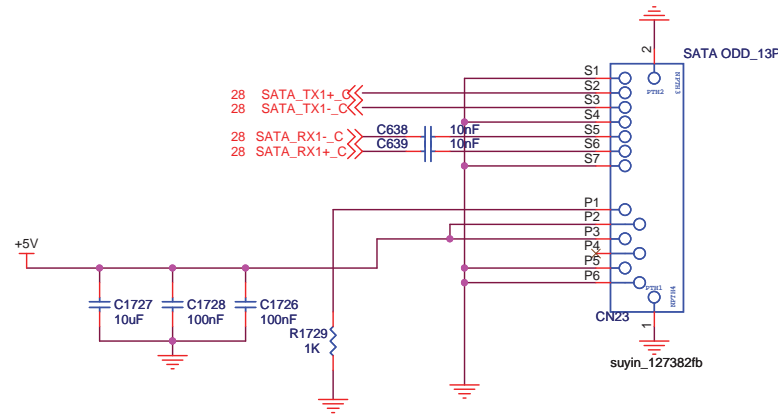





## SATA HDD Conn.



To support Mobile SATA ODD through cable

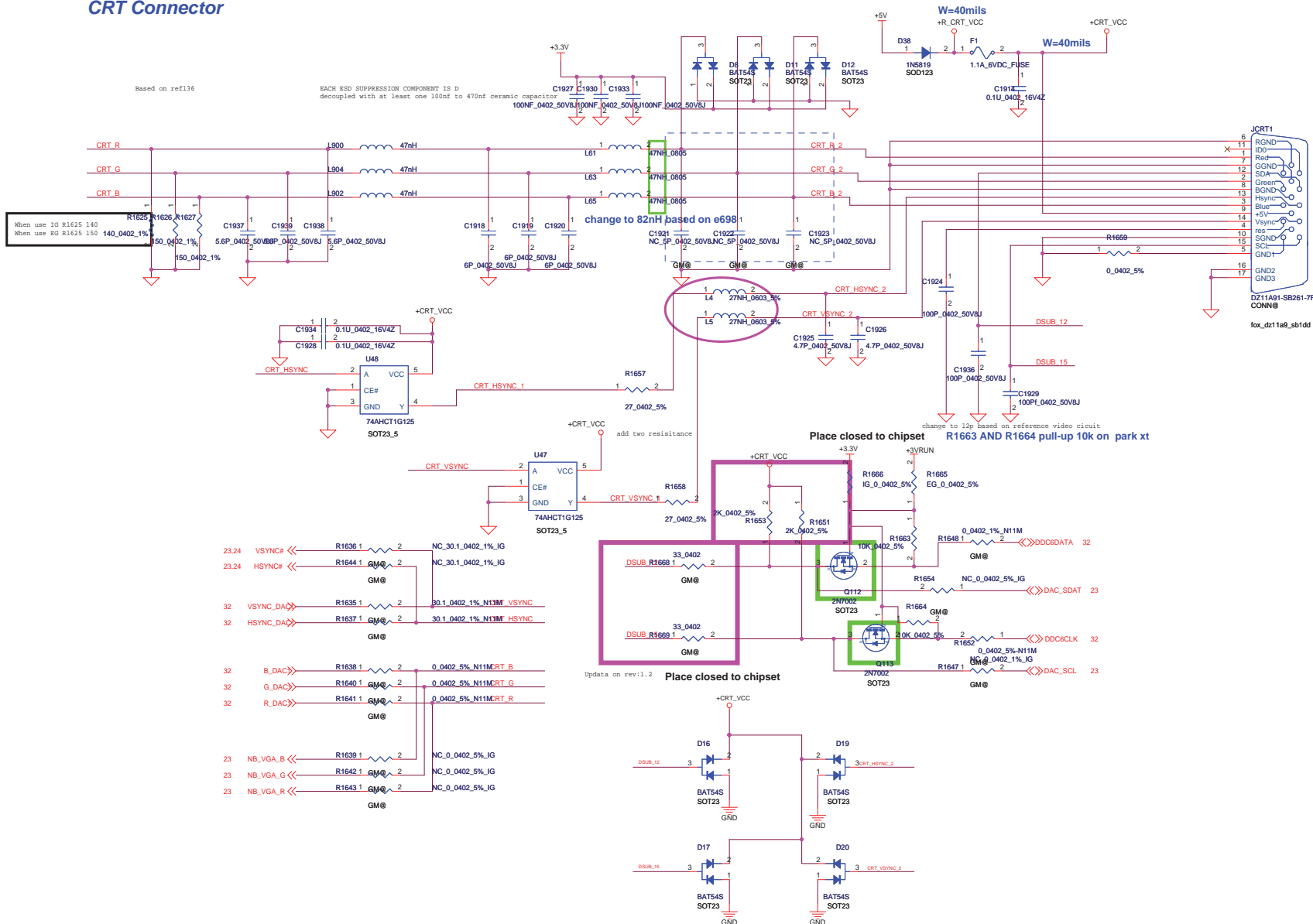


		Bitland Information Technology Co., Ltd. Notebook R&D Division	
Title		SATA HDD /ODD	
Size B	Document Number	BM5016	Rev 1.0
Date:	Thursday, August 05, 2010	Sheet 41 of 54	



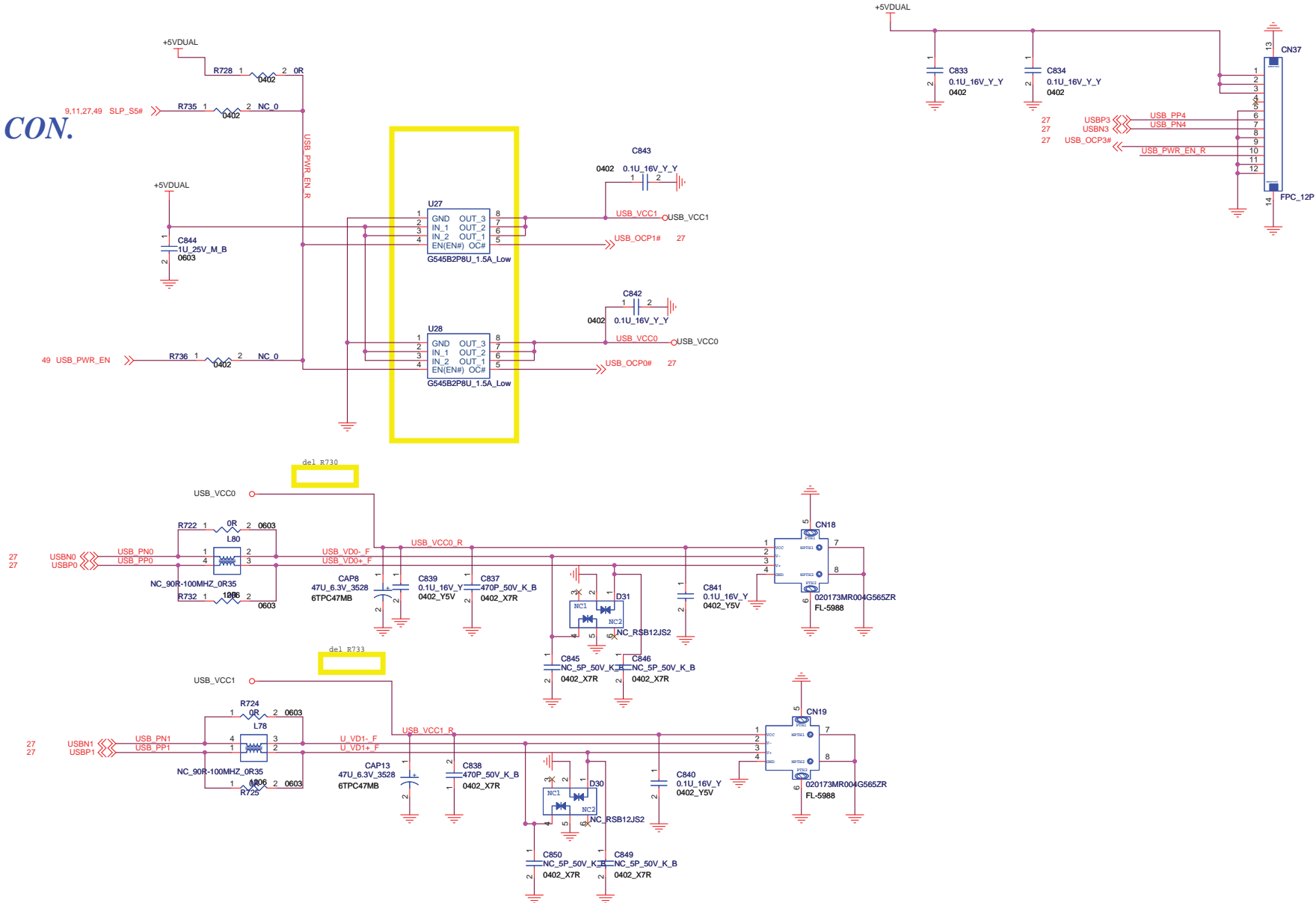


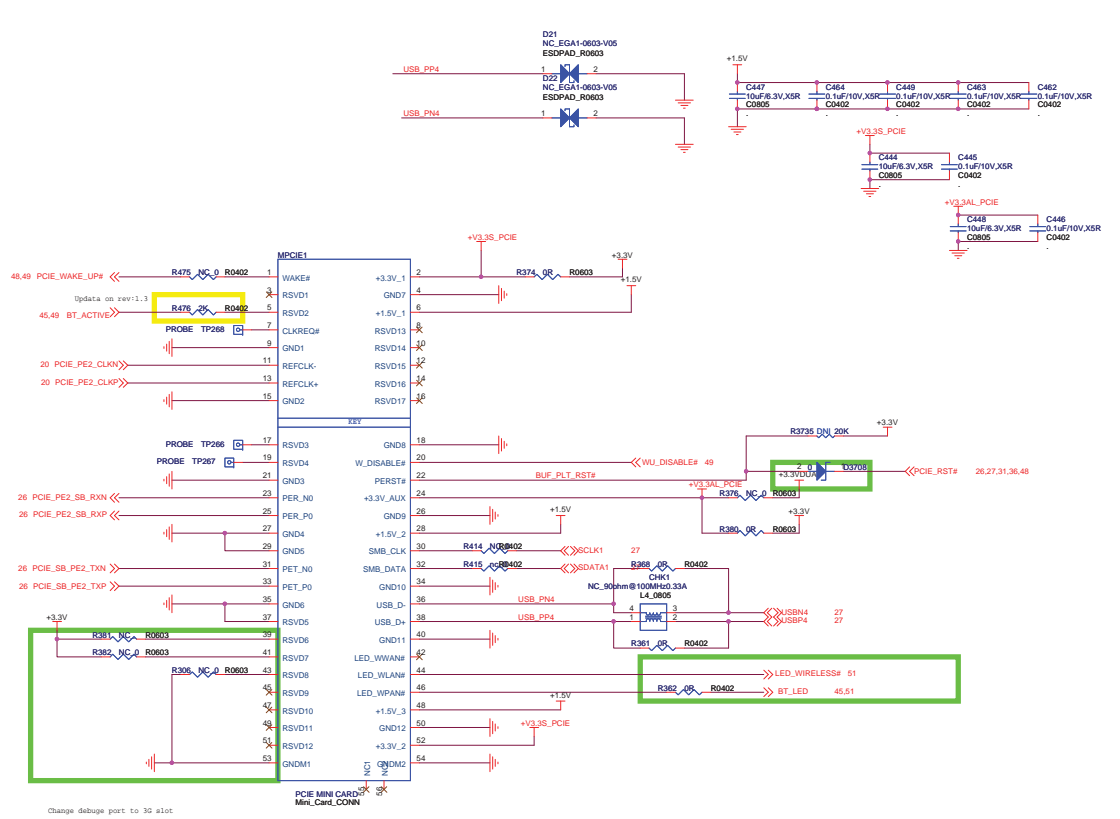
### CRT Connector





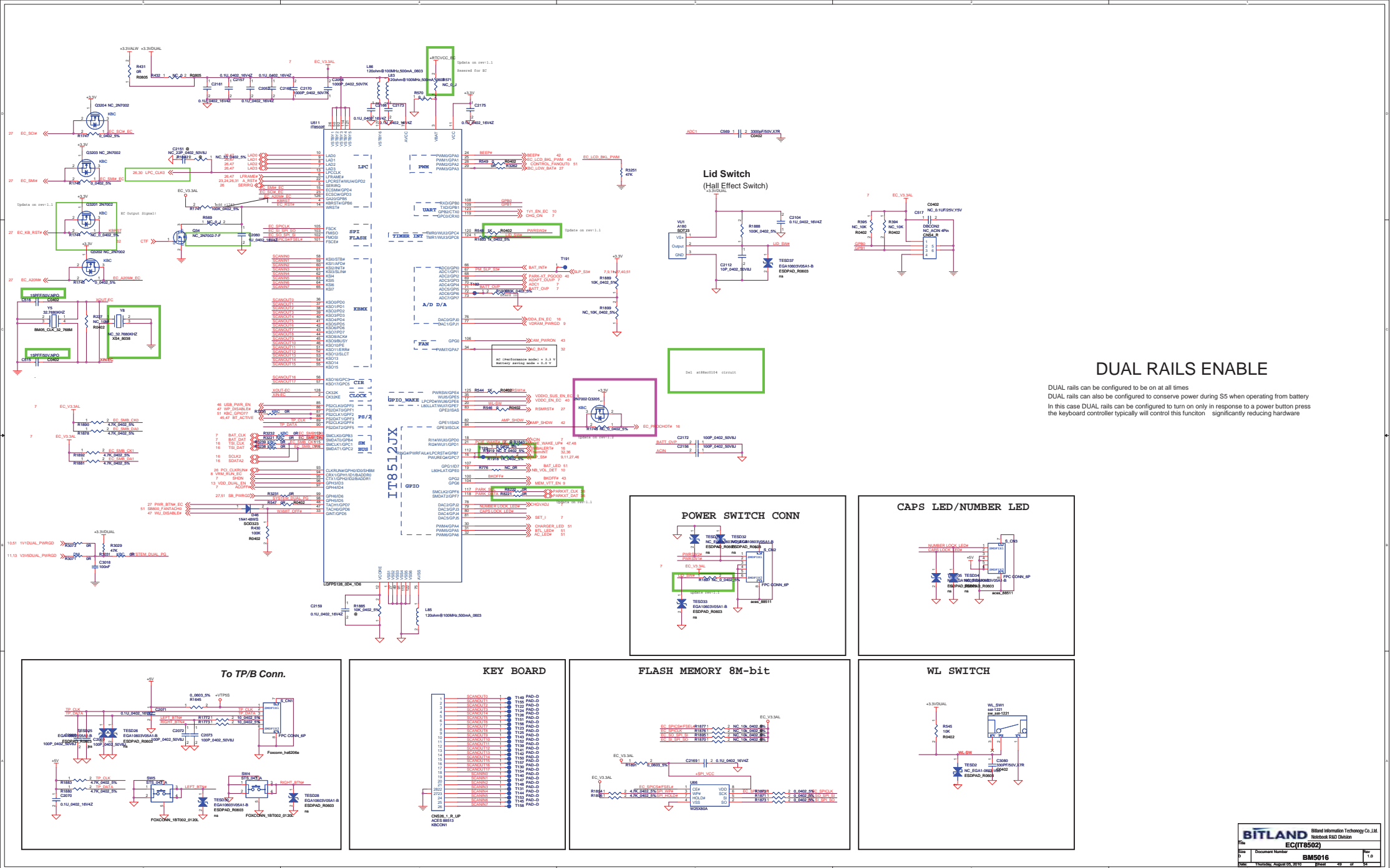
# USB CON.












5	4	3	2	1
D				
C				
B				
A				



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Title

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Date: Thursday, August 05, 2010

Sheet 50 of 54

BM5016







